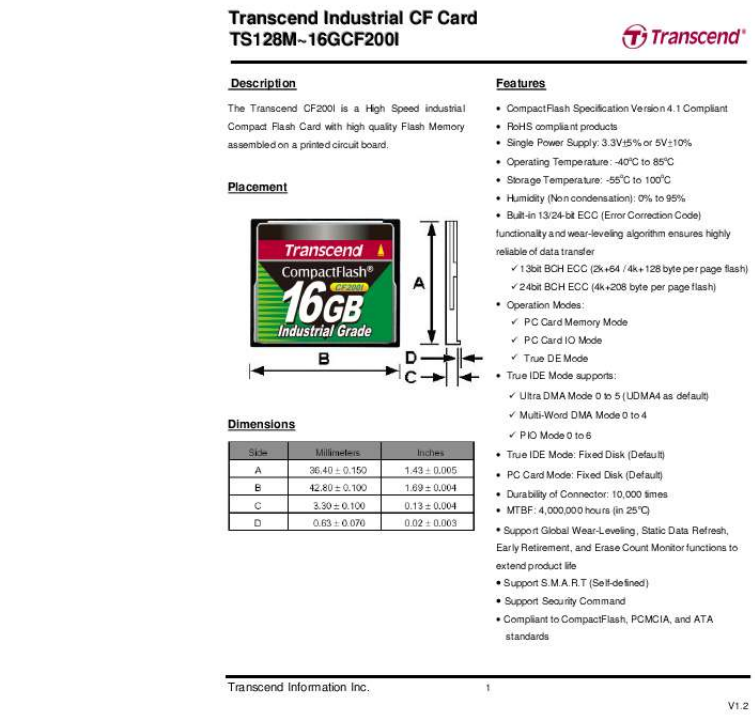

Transcend Industrial CF Card
TS128M~16GCF200I

Transcend

Description

The Transcend CF200I is a High Speed industrial Compact Flash Card with high quality Flash Memory assembled on a printed circuit board.

Placement

Dimensions

Side	Millimeters	Inches
A	36.40 ± 0.150	1.43 ± 0.005
B	42.80 ± 0.100	1.69 ± 0.004
C	3.30 ± 0.100	0.13 ± 0.004
D	0.63 ± 0.076	0.02 ± 0.003

Features

- CompactFlash Specification Version 4.1 Compliant
- RoHS compliant products
- Single Power Supply: 3.3V±5% or 5V±10%
- Operating Temperature: -40°C to 85°C
- Storage Temperature: -55°C to 100°C
- Humidity (Non condensation): 0% to 95%
- Built-in 13/24-bit ECC (Error Correction Code) functionality and wear-leveling algorithm ensures highly reliable of data transfer
  - ✓ 13bit BCH ECC (2k+64 / 4k+128 byte per page flash)
  - ✓ 24bit BCH ECC (4k+208 byte per page flash)
- Operation Modes:
  - ✓ PC Card Memory Mode
  - ✓ PC Card IO Mode
  - ✓ True DE Mode
- True IDE Mode supports:
  - ✓ Ultra DMA Mode 0 to 5 (UDMA4 as default)
  - ✓ Multi-Word DMA Mode 0 to 4
  - ✓ PIO Mode 0 to 6
- True IDE Mode: Fixed Disk (Default)
- PC Card Mode: Fixed Disk (Default)
- Durability of Connector: 10,000 times
- MTBF: 4,000,000 hours (in 25°C)
- Support Global Wear-Leveling, Static Data Refresh, Early Retirement, and Erase Count Monitor functions to extend product life
- Support S.M.A.R.T (Self-defined)
- Support Security Command
- Compliant to CompactFlash, PCMCIA, and ATA standards

Transcend Information Inc. 1

V1.2

Manual abstract:

StandBy Current : 5V : 2.8mA 3.3V : 2.2mA 3. @@@@(2) Find the static-block and save it in wear-leveling pointer. (3) Check the erase count when the block popped from spare pool. If the block erase count is bigger than WEARCNT, then swapped the static-block and over-count-block. After actual test, global wear leveling successfully even the erase count of every block; hence, it can extend the life expectancy of Flash product. 2. StaticDataRefresh Technology Keeping Data Healthy There are many variants that would disturb the charge inside a Flash cell.

These variants can be: time, read operations, undesired charge, heat, etc; each variant would create a charge loss, and the contents shift in their charge levels slightly. In our everyday usage more than 60% are repeated read operations, the accumulated charge loss would eventually result in the data loss. Normally, ECC engine corrections are taken place without affecting the host normal operations. As time passes by, the number of error bits accumulated in the read transaction exceeds the correcting capability of the ECC engine, resulting in corrupted data being sent to the host. To prevent this, Transcend's CF200I monitor the error bit levels at each read operation; when it reaches the preset threshold value, the controller automatically performs data refresh to "restore" the correct charge levels in the cell.

This implementation practically restores the data to its original, error-free state, and hence, lengthening the life of the data. 3. EarlyRetirement Avoiding Data Loss Due to Weak Block The StaticDataRefresh feature functions well when the cells in a block are still healthy. As the block ages over time, it cannot store charge reliably anymore, EarlyRetirement enters the scene. EarlyRetirement works by moving the static data to another block (a health block) before the previously used block becomes completely incapable of holding charges for data.

When the charge loss error level exceeds another threshold value (higher from that for StaticDataRefresh), the controller automatically moves its data to another block. In addition, the original block is then marked as a bad block, which prevents its further use, and thus the block enters the state of "EarlyRetirement." Note that, through this process, the incorrect data are detected and effectively corrected by the ECC engine, thus the data in the new block is stored error-free. Transcend Information Inc. 4 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Transcend Transcend Information Inc. 5 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Block Diagram Transcend Information Inc. 6 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Pin Assignments and Pin Type Transcend Information Inc.

7 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Note: 1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current. 2) The signal should be grounded by the host. 3) The signal should be tied to VCC by the host. 4) The mode is required for CompactFlash Storage Cards. 5) The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled upon the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host. 6) If DMA operations are not used, the signal should be held high or tied to VCC by the host.

For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal,including a floating condition 7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active. 8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active. 9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active. 10) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Write is active. 11) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Read is active.

12) Signal usage in PC Card I/O and Memory Mode when Ultra DMA protocol is active. Transcend Information Inc. 8 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Signal Description Signal Name A10 A00 (PC Card Memory Mode) Dir. I Pin Description 8,10,11,12, These address lines along with the -REG signal are used to select the following: 14,15,16,17, The I/O port address registers within the CompactFlash Storage Card , the memory mapped port address registers within the CompactFlash Storage Card, 18,19,20 a byte in the card's information structure and its configuration control and status registers.

This signal is the same as the PC Card Memory Mode signal. A10 A00 (PC Card I/O Mode) A02 - A00 (True IDE Mode) I 18,19,20 In True IDE Mode, only A[02:00] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host. This signal is asserted high, as BVD1 is not supported. BVD1 (PC Card Memory Mode) -STSCHG (PC Card I/O Mode) Status Changed -PDIAG (True IDE Mode) BVD2 (PC Card Memory Mode) -SPKR (PC Card I/O Mode) -DASP (True IDE Mode) -CD1, -CD2 (PC Card Memory Mode) I/O 46 This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register. In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol. I/O 45 This signal is asserted high, as BVD2 is not supported. This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated. In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.

O 26,25 These Card Detect pins are connected to ground on the CompactFlash Storage Card. They are used by the host to determine that the CompactFlash Storage Card is fully inserted into its socket. This signal is the same for all modes. -CD1, -CD2 (PC Card I/O Mode) -CD1, -CD2 (True IDE Mode) This signal is the same for all modes. Transcend Information Inc. 9 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Signal Name -CE1, -CE2 (PC Card Memory Mode) Card Enable Dir. I Pin 7,32 Description These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word.-CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2.

A multiplexing scheme based on A0,-CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Table 27, Table 29, Table 31, Table 35, Table 36 and Table 37. This signal is the same as the PC Card Memory Mode signal. -CE1, -CE2 (PC Card I/O Mode) Card Enable -CS0, -CS1 (True IDE Mode) In the True IDE Mode, -CS0 is the address range select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While DMACK is asserted, -CS0 and CS1 shall be held negated and the width of the transfers shall be 16 bits.

-CSEL (PC Card Memory Mode) -CSEL (PC Card I/O Mode) -CSEL (True IDE Mode) I 39 This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.

D15 - D00 (PC Card Memory Mode) I/O 31,30,29,28, These lines carry the Data, Commands and Status information between the host 27,49,48,47, and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB 6,5,4,3,2, of the Odd Byte of the Word. 23, 22, 21 This signal is the same as the PC Card Memory Mode signal. DMode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol. In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst. STOP (True IDE Mode - Ultra DMA Protocol Active) -OE (PC Card Memory Mode) I 9 This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.

To enable True IDE Mode this input should be grounded by the host. -OE (PC Card I/O Mode) -ATA SEL (True IDE Mode) READY (PC Card Memory Mode) O 37 In Memory Mode, this signal is set high when the CompactFlash Storage Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state. -IREQ (PC Card I/O Mode) I/O Operation After the CompactFlash Storage Card Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE Mode signal is the active high Interrupt Request to the host. INTRQ (True IDE Mode)

This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the -DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes. RESET (PC Card Memory Mode) I 41 The CompactFlash Storage Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card.

Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Storage Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set. RESET (PC Card I/O Mode) -RESET (True IDE Mode) VCC (PC Card Memory Mode) VCC (PC Card I/O Mode) VCC (True IDE Mode) This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, this input pin is the active low hardware reset from the host. -- 13,38 +5 V, +3.3 V power. This signal is the same for all modes. This signal is the same for all modes. Transcend Information Inc. 13 V1.

The device may negate -DDMARDY to pause an Ultra DMA transfer. In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst. DSTROBE (True IDE Mode Ultra DMA Read Mode) -WE (PC Card Memory Mode) I 36 This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card when the card is configured in the memory interface mode.

It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. -WE (PC Card I/O Mode) -WE (True IDE Mode) WP (PC Card Memory Mode) Write Protect -IOIS16 (PC Card I/O Mode) O 24 In True IDE Mode, this input signal is not used and should be connected to VCC by the host. Memory Mode The CompactFlash Storage Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.

I/O Operation When the CompactFlash Storage Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle. -IOCS16 (True IDE Mode) Transcend Information Inc. 14 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Electrical Specification The following tables indicate all D.C. Characteristics for the CompactFlash Storage Card. Unless otherwise stated, conditions are: Vcc = 5V ±10% Vcc = 3.3V ± 5% Absolute Maximum Conditions Input Power Input Leakage Current Input Characteristics CompactFlash interface I/O at 5.

0V Parameter Supply Voltage High level output voltage Low level output voltage High level input voltage Low level input voltage Pull up resistance 2 Symbol VCC VOH VOL VIH VIL RPU RPD Min. 4.5 VCC-0.8 Max. 5.5 0.8 Unit V V V V V Remark 4.0 2.92 0.8 1.

70 50. 50 73 97 Non-schmitt trigger Schmitt trigger Schmitt trigger 1 V V kOhm kOhm Non-schmitt trigger 1 Pull down resistance Transcend Information Inc. 15 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 CompactFlash interface I/O at 3.3V Parameter Supply Voltage High level output voltage Low level output voltage High level input voltage Low level input voltage Pull up resistance 2 Symbol VCC VOH VOL VIH VIL RPU RPD Min.

2.97 VCC-0.8 Max. 3.63 0.

8 Unit V V V V V Remark 2.4 2.05 0.6 1.25 52.7 47.5 141 172 Non-schmitt trigger Schmitt trigger Schmitt trigger 1 V V kOhm kOhm Non-schmitt trigger 1 Pull down resistance The I/O pins other than CompactFlash interface Parameter Supply Voltage High level output voltage Low level output voltage High level input voltage Low level input voltage Pull up resistance Pull down resistance Symbol VCC VOH VOL VIH VIL RPU RPD 2.0 1.4 0.8 40 40 2.

0 0.8 1.2 Min. 2.7 2.4 0.4 Max. 3.6 Unit V V V V V V V kOhm kOhm Non-schmitt trigger Schmitt trigger Non-schmitt trigger Schmitt trigger Remark 1. Include CE1, CE2, HREG, HOE.

HIOE, HWE, HIOW pins. 2. Include CE1, CE2, HREG, HOE. HIOE, HWE, HIOW, CSEL, PDIAG, DASP pins. Transcend Information Inc. 16 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Output Drive Type Output Drive Characteristics Transcend Information Inc. 17 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Signal Interface Transcend Information Inc. 18 V1.

2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Notes: 1) Control Signals: each card shall present a load to the socket no larger than 50 pF 10 at a DC current of 700 A low state and 150 A high state, including pull-resistor. The socket shall be able to drive at least the following load 10 while meeting all AC timing requirements: (the number of sockets wired in parallel) multiplied by (50 pF with DC current 700 A low state and 150 A high state per socket). 2) Resistor is optional. 3) Status Signals: the socket shall present a load to the card no larger than 50 pF 10 at a DC current of 400 A low 10 while meeting all AC timing requirements: 50 pF at a DC current of 400 A low state and 1100 A high state. 6) BVD2 was not defined in the JEIDA 3.0 release. Systems fully supporting JEIDA release 3 SRAM cards shall pull-up pin 45 (BVD2) to avoid sensing their batteries as "Low." 7) Address Signals: each card shall present a load of no more than 100pF 10 at a DC current of 450 A low state and 150 A high state. The host shall be able to drive at least the following load 10 while meeting all AC timing requirements: (the number of sockets wired in parallel) multiplied by (100pF with DC current 450 A low state and 150 A high state per socket). 8) Data Signals: the host and each card shall present a load no larger than 50pF 10 at a DC current of 450 A and 150 A high state.

The host and each card shall be able to drive at least the following load 10 while meeting all AC timing requirements: 100pF with DC current 1.6mA low state and 300 A high state. This permits the host to wire two sockets in parallel without derating the card access speeds. 9) Reset Signal: This signal is pulled up to prevent the input from floating when a CFA to PCMCIA adapter is used in a PCMCIA revision 1 host. However, to minimize DC current drain through the pull-up resistor in normal operation the pull-up should be turned off once the Reset signal has been actively driven low by the host. Consequently, the input is specified as an I2Z because the resistor is not necessarily detectable in the input current leakage test. 10) Host and card restrictions for CF Advanced Timing Modes and Ultra DMA modes: Additional Requirements for CF Advanced Timing Modes and Ultra DMA Electrical Requirements for additional required limitations on the implementation of CF Advanced Timing modes and Ultra DMA modes respectively. Additional Requirements for CF Advanced Timing Modes The CF Advanced Timing modes include PCMCIA I/O and Memory modes that are 100ns or faster and True IDE PIO Modes 5,6 and Multiword DMA Modes 3,4. When operating in CF Advanced timing modes, the host shall conform to the following requirements: 1) Only one CF device shall be attached to the CF Bus. 2) The host shall not present a load of more than 40pF to the device for all signals, including any cabling.

3) The maximum cable length is 0.15 m (6 in). The cable length is measured from the card connector to the host controller. 0.46 m (18 in) cables are not supported.

4) The -WAIT and IORDY signals shall be ignored by the host. Devices supporting CF Advanced timing modes shall also support slower timing modes, to ensure operability with systems that do not support CF Advanced timing modes Transcend Information Inc. 19 V1.2 state and 100 A high state, including pull-up resistor. The card shall be able to drive at least the following load 5) Status Signals: the socket shall present a load to the card no larger than 50 pF 10 at a DC current of 400 10 while meeting all AC timing requirements: 50 pF at a DC current of 400 state and 100 A high state, including pull-up resistor.

The card shall be able to drive at least the following load A low state and 100 A high state. A low 4) Status Signals: the socket shall present a load to the card no larger than 50 pF 10 at a DC current of 400 10 while meeting all AC timing requirements: 50 pF at a DC current of 400 state and 100 A high state, including pull-up resistor. The card shall be able to drive at least the following load A low state and 100 A high state. A low Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Ultra DMA Electrical Requirements Host and Card signal capacitance limits for Ultra DMA operation The host interface signal capacitance at the host connector shall be a maximum of 25 pF for each signal as measured at 1 MHz. The card interface signal capacitance at the card connector shall be a maximum of 20 pF for each signal as measured at 1 MHz. Series termination required for Ultra DMA operation Series termination resistors are required at both the host and the card for operation in any of the Ultra DMA modes. Table 13 describes typical values for series termination at the host and the device. Signal Table: Typical Series Termination for Ultra DMA Transcend Information Inc. 20 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Table: Ultra DMA Termination with Pull-up or Pull down Example Printed Circuit Board (PCB) Trace Requirements for Ultra DMA On any PCB for a host or device supporting Ultra DMA: The longest D[15:00] trace shall be no more than 0.

5" longer than either STROBE trace as measured from the IC pin to the connector. The shortest D[15:00] trace shall be no more than 0.5" shorter than either STROBE trace as measured from the IC pin to the connector. Ultra DMA Mode Cabling Requirement Operation in Ultra DMA mode requires a crosstalk suppressing cable. The cable shall have a grounded line between each signal line. For True IDE mode operation using a cable with IDE (ATA) type 40 pin connectors it is recommended that the host sense the cable type using the method described in the ANSI INCITS 361-2002 AT Attachment - 6 standard, to prevent use of Ultra DMA with a 40 conductor cable. Transcend Information Inc. 21 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Attribute Memory Read Timing Specification Transcend Information Inc. 22 V1.
2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Configuration Register (Attribute Memory) Write Timing Specification Transcend Information Inc. 23 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Common Memory Read Timing Specification Transcend Information Inc. 24 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Common Memory Write Timing Specification Transcend Information Inc.
25 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 I/O Input (Read) Timing Specification Transcend Information Inc. 26 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 I/O Output (Write) Timing Specification Transcend Information Inc. 27 V1.
2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Transcend Information Inc. 28 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 True IDE PIO Mode Read/Write Timing Specification Transcend Information Inc. 29 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Transcend Information Inc. 30 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Transcend Information Inc. 31 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 True IDE Ultra DMA Mode Read/Write Timing Specification Table: Ultra DMA Data Burst Timing Transcend Information Inc. 32 V1.

2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Notes: 1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V. 2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and DMARDY transitions are measured at the sender connector. 3) The parameter tCYC shall be measured at the recipient's connector farthest from the sender. 4)The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector. 5)The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus the allow for a bus turnaround. Transcend Information Inc. 33 V1.
2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Transcend Information Inc. 34 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Notes: 1) The parameters tUI, tMLI : (Ultra DMA Data-In Burst Device Termination Timing and Ultra DMA Data-In Burst Host Termination Timing), and tLI indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding.
tUI is an unlimited interlock that has no maximum time value. tMLI is a limited time-out that has a defined minimum. tLI is a limited time-out that has a defined maximum. 2) 80-conductor cabling shall be required in order to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes greater than 2. 3) Timing for tDVS, tDVH, tCVS and tCVH shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value.
Due to reflections on the cable, these timing measurements are not valid in a normally functioning system. 4)For all modes the parameter tZIORDY may be greater than tENV due to the fact that the host has a pull-up on IORDY- giving it a known state when released. 5)The parameters tDS, and tDH for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for tDS and tDH for mode 5 at the middle connector being 3.0 and 3.9 ns respectively. 6)The parameters are applied to True IDE mode operationonly. Table: Ultra DMA Sender and Recipient IC Timing Requirements Notes: 1) All timing measurement switching points(low to high and high to low) shall be taken at 1.

5 V. 2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.

4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V). 3) The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values. Transcend Information Inc. 35 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Table: Ultra DMA Sender and Recipient IC Timing Requirements Note: 1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector. The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.
05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values. Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.
Transcend Information Inc. 36 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Card Configuration The CompactFlash Storage Cards is identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the CompactFlash Storage Card that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards. Multiple Function CompactFlash Storage Cards Table: CompactFlash Storage Card Registers and Memory Space Decoding Table: CompactFlash Storage Card Configuration Registers Decoding Transcend Information Inc. 37 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Attribute Memory Function Attribute memory is a space where CompactFlash Storage Card identification and configuration information are stored, and is limited to 8 bit wide accesses only at even addresses. The card configuration registers are also located here. For CompactFlash Storage Cards, the base address of the ard configuration registers is 200h.

Table 31: Attribute Memory Function Transcend Information Inc. 38 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Configuration Option Register (Base + 00h in Attribute Memory) Transcend Information Inc. 39 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Card Configuration and Status Register (Base + 02h in Attribute Memory) Transcend Information Inc. 40 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Pin Replacement Register (Base + 04h in Attribute Memory) Transcend Information Inc. 41 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Socket and Copy Register (Base + 06h in Attribute Memory) Transcend Information Inc. 42 V1.
2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 I/O Transfer Function The I/O transfer to or from the CompactFlash Storage can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash Storage. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash Storage, the system shall generate a pair of 8 bit references to access the word ѐ even byte and odd byte. The CompactFlash Storage Card permits both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash Storage responds.
The CompactFlash Storage Card may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle. Table : PCMCIA Mode I/O Function Transcend Information Inc. 43 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Common Memory Transfer Function The Common Memory transfer to or from the CompactFlash Storage can be either 8 or 16 bits. Table: Common Memory Function Transcend Information Inc.
44 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 True IDE Mode I/O Transfer Function The CompactFlash Storage Card can be configured in a True IDE Mode of operation. The CompactFlash Storage Card is configured in this mode only when the -OE input signal is grounded by the host during the power off to power on cycle. Optionally, CompactFlash Storage Cards may support the following optional detection methods: 1. The card is permitted to monitor the OE (-ATA SEL) signal at any time(s) and switch to PCMCIA mode upon detecting a high level on the pin. 2. The card is permitted to re-arbitrate the interface mode determination following a transition of the (-)RESET pin. 3. The card is permitted to monitor the OE (-ATA SEL) signal at any time(s) and switch to True IDE mode upon detection of a continuous low level on pin for an extended period of time. Table: True IDE Mode I/O Function defines the function of the operations for the True IDE Mode.

Transcend Information Inc. 45 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Metaformat Overview The goal of the Metaformat is to describe the requirements and capabilities of the CompactFlash Storage Card as thoroughly as possible. This includes describing the power requirements, IO requirements, memory requirements, manufacturer information and details about the services provided.

Table: Sample Device Info Tuple Information for Extended Speeds Note: The value "1" defined for D3 of the N+0 words indicates that no write-protect switch controls writing the ATA registers. The value "0" defined for D7 in the N+2 words indicates that there is not more than a single speed extension byte. Transcend Information Inc. 46 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 CF-ATA Drive Register Set Definition and Protocol The CompactFlash Storage Card can be configured as a high performance I/O device through: a) The standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary) or 170h- 177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ). b) Any system decoded 16 byte I/O block using any available IRQ.

c) Memory space. The communication to or from the CompactFlash Storage Card is done using the Task File registers, which provide all the necessary registers for control and status information related to the storage medium. The PCMCIA interface connects peripherals to the host using four register mapping methods. Table 39 is a detailed description of these methods: Transcend Information Inc. 47 V1.

2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 I/O Primary and Secondary Address Configurations Table: Primary and Secondary I/O Decoding Transcend Information Inc. 48 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Contiguous I/O Mapped Addressing When the system decodes a contiguous block of I/O registers to select the CompactFlash Storage Card, the registers are accessed in the block of I/O space decoded by the system as follows: Table: Contiguous I/O Decoding Transcend Information Inc. 49 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Memory Mapped Addressing When the CompactFlash Storage Card registers are accessed via memory references, the registers appear in the common memory space window: 0-2K bytes as follows: True IDE Mode Addressing When the CompactFlash Storage Card is configured in the True IDE Mode, the I/O decoding is as follows: Transcend Information Inc.

50 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 CF-ATA Registers The following section describes the hardware registers used by the host software to issue commands to the CompactFlash device. These registers are often collectively referred to as the "task file." Data Register (Address - 1F0h[170h];Offset 0,8,9) The Data Register is a 16 bit register, and it is used to transfer data blocks between the CompactFlash Storage Card data buffer and the Host. This register overlaps the Error Register. Error Register (Address - 1F1h[171h]; Offset 1, 0Dh Read Only) This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. This register is also accessed in PC Card Modes on data bits D15-D8 during a read operation to offset 0 with -CE2 low and -CE1 high. Bit 7 (BBK/ICRC): this bit is set when a Bad Block is detected. This bit is also set when an interface CRC error is detected in True IDE Ultra DMA modes of operation. Bit 6 (UNC): this bit is set when an Uncorrectable Error is encountered.

Bit 5: this bit is 0. Bit 4 (IDNF): the requested sector ID is in error or cannot be found. Bit 3: this bit is 0. Bit 2 (Abort) This bit is set if the command has been aborted because of a CompactFlash Storage Card status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued. Bit 1 This bit is 0. Bit 0 (AMNF) This bit is set in case of a general error. Transcend Information Inc. 51 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Feature Register (Address - 1F1h[171h]; Offset 1, 0Dh Write Only) This register provides information regarding features of the CompactFlash Storage Card that the host can utilize.

This register is also accessed in PC Card modes on data bits D15-D8 during a write operation to Offset 0 with -CE2 low and -CE1 high. Sector Count Register (Address - 1F2h[172h]; Offset 2) This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the CompactFlash Storage Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

Sector Number (LBA 7-0) Register (Address - 1F3h[173h]; Offset 3) This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any CompactFlash Storage Card data access for the subsequent command. 6.1.5.5 Cylinder Low (LBA 15-8) Register (Address - 1F4h[174h]; Offset 4) This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

Cylinder High (LBA 23-16) Register (Address - 1F5h[175h]; Offset 5) This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address. Drive/Head (LBA 27-24) Register (Address 1F6h[176h]; Offset 6) The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. Bit 7: this bit is specified as 1 for backward compatibility reasons. It is intended that this bit will become obsolete in a future revision of the specification. This bit is ignored by some controllers in some commands. Bit 6: LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows: LBA7-LBA0: Sector Number Register D7-D0.

LBA15-LBA8: Cylinder Low Register D7-D0. LBA23-LBA16: Cylinder High Register D7-D0. LBA27-LBA24: Drive/Head Register bits HS3-HS0. Bit 5: this bit is specified as 1 for backward compatibility reasons. It is intended that this bit will become obsolete in a future revisions of the specification. This bit is ignored by some controllers in some commands. Bit 4 (DRV): DRV is the drive number. When DRV=0, drive (card) 0 is selected. When DRV=1, drive (card) 1 is selected. Setting this bit to 1 is obsolete in PCMCIA modes of operation.

If the obsolete functionality is support by a CF Storage Card, the CompactFlash Storage Card is set to be Card 0 or 1 using the copy field (Drive #) of the PCMCIA Socket & Copy configuration register. Transcend Information Inc. 52 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Bit 3 (HS3): when operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number.

It is Bit 27 in the Logical Block Address mode.

Bit 2 (HS2): when operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode. Bit 1 (HS1): when operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode. Bit 0 (HS0): when operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number.

It is Bit 24 in the Logical Block Address mode. Status & Alternate Status Registers (Address 1F7h[177h]&3F6h[376h]; Offsets 7 & Eh) These registers return the CompactFlash Storage Card status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The status bits are described as follows: Bit 7 (BUSY): the busy bit is set when the CompactFlash Storage Card has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1. During the data transfer of DMA commands, the Card shall not assert DMARQ unless either the BUSY bit, the DRQ bit, or both are set to one. Bit 6 (RDY): RDY indicates whether the device is capable of performing CompactFlash Storage Card operations. This bit is cleared at power up and remains cleared until the CompactFlash Storage Card is ready to accept a command. Bit 5 (DWF): This bit, if set, indicates a write fault has occurred. Bit 4 (DSC): This bit is set when the CompactFlash Storage Card is ready.

Bit 3 (DRQ): The Data Request is set when the CompactFlash Storage Card requires that information be transferred either to or from the host through the Data register. During the data transfer of DMA commands, the Card shall not assert DMARQ unless either the BUSY bit, the DRQ bit, or both are set to one. Bit 2 (CORR): This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation. Bit 1 (IDX): This bit is always set to 0. Bit 0 (ERR): This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. It is recommended that media access commands (such as Read Sectors and Write Sectors) that end with an error condition should have the address of the first sector in error in the command block registers. Transcend Information Inc. 53 V1.

2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Device Control Register (Address - 3F6h[376h]; Offset Eh) This register is used to control the CompactFlash Storage Card interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY. The bits are defined as follows: Bit 7: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0. Bit 6: this bit is ignored by the CompactFlash Storage Card.

The host software should set this bit to 0. Bit 5: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0. Bit 4: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0.

Bit 3: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0. Bit 2 (SW Rst): this bit is set to 1 in order to force the CompactFlash Storage Card to perform an AT Disk controller Soft Reset operation. This does not change the PCMCIA Card Configuration Registers as a hardware Reset does. @@@@@@This bit is set to 0 at power on and Reset. @@@@@@@@@@@@@@@@@@@@@@@@@@@@@Bit 1 (-nDS1): this bit is 0 when drive 1 is active and selected. @@@@@@@@The card returns status with RDY=1 and DSC=1 after the data in the write cache buffer is written to the media. If the Compact Flash Storage Card does not support the Flush Cache command, the Compact Flash Storage Card shall return command aborted. Identify Device ECh The Identify Device command enables the host to receive parameter information from the CompactFlash Storage Card. This command has the same protocol as the Read Sector(s) command.

The parameter words in the buffer have the arrangement and meanings defined in Table as below. All reserved bits or words are zero. Hosts should not depend on Obsolete words in Identify Device containing 0. Table 47 specifies each field in the data returned by the Identify Device Command. In Table as below, X indicates a numeric nibble value specific to the card and aaaa indicates an ASCII string specific to the particular drive. Read DMA C8h Read Multiple - C4h Transcend Information Inc. 63 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Read Sector(s) - 20h or 21h Read Verify Sector(s) - 40h or 41h Set Multiple Mode - C6h Write DMA CAh Transcend Information Inc. 64 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Write Multiple Command - C5h Write Sector(s) - 30h or 31h NOP - 00h This command always fails with the CompactFlash Storage Card returning command aborted.

Transcend Information Inc. 65 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Read Buffer - E4h The Read Buffer command enables the host to read the current contents of the CompactFlash Storage Card's sector buffer. This command has the same protocol as the Read Sector(s) command. Write Buffer - E8h Check Power Mode - 98h or E5h If the CompactFlash Storage Card is in, going to, or recovering from the sleep mode, the CompactFlash Storage Transcend Information Inc.

66 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt. If the CompactFlash Storage Card is in Idle mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt. Idle - 97h or E3h This command causes the CompactFlash Storage Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled.

If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification. Idle Immediate - 95h or E1h This command causes the CompactFlash Storage Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. Set Sleep Mode- 99h or E6h Transcend Information Inc. 67 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Standby - 96h or E2h Standby Immediate - 94h or E0h Security Set Password F1h Transcend Information Inc.

68 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Table Security Unlock F2h Security Erase Prepare F3h Transcend Information Inc. 69 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Security Erase Unit F4h Security Freeze Lock F5h Transcend Information Inc.

70 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Security Freeze Lock F6h Format Track - 50h This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the CompactFlash Storage Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the CompactFlash Storage Card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended. Initialize Drive Parameters - 91h This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command. Recalibrate - 1Xh Transcend Information Inc. 71 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Seek - 7Xh Wear Level - F5h Write Verify - 3Ch Error Posting Transcend Information Inc.
72 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Transcend Information Inc. 73 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Error and Status Register summarizes the valid status and error value for all the CF-ATA Command set. Transcend Information Inc.
74 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 ID Table Information of True IDE Mode Word Address 0 1 2 3 4 5 6 7-8 9 10-19 20 21 22 23-26 27-46 47 48 49 50 51 52 53 54 55 56 57-58 59 60-61 62 63 64 65 66 Default Value 044Ah 0XXX XXXXh 0000h 00XXh 0000h 0240h XXXXh XXXXh 0000h aaaa 0000h 0002h 0004h aaaa aaaa 8001h 0000h 0F00h 0000h 0200h 0000h 0007h XXXXh XXXXh XXXXh XXXXh 01XXh XXXXh 0000h 0007h 0003h 0078h 0078h Total Bytes 2 2 2 2 2 2 2 2 4 2 20 2 2 2 8 40 2 2 2 2 2 2 2 2 2 2 4 2 4 2 2 2 2 2 Data Field Type Information General configuration - signature for the CompactFlash Flash Storage Card General configuration Bit Significant with ATA-4 definitions. Default number of cylinders Reserved Default number of heads Obsolete Obsolete Default number of sectors per track Number of sectors per card (Word 7 = MSW, Word 8 = LSW) Obsolete Serial number in ASCII (Right Justified) Obsolete Obsolete Number of ECC bytes passed on Read/Write Long Commands Firmware revision in ASCII. Big Endian Byte Order in Word Model number in ASCII (Left Justified) Big Endian Byte Order in Word Maximum number of sectors on Read/Write Multiple command Reserved Capabilities Reserved PIO data transfer cycle timing mode Obsolete Field Validity Current numbers of cylinders Current numbers of heads Current sectors per track Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW) Multiple sector setting Total number of sectors addressable in LBA Mode Reserved Multiword DMA transfer. In PC Card modes this value shall be 0h Advanced PIO modes supported Minimum Multiword DMA transfer cycle time per word.
In PC Card modes this value shall be 0h Recommended Multiword DMA transfer cycle time. In PC Card modes this value shall be 0h Transcend Information Inc. 75 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Word Address 67 68 69-79 80-81 82-84 83 84 85-87 88 89 90 91 92 93 94-127 128 129-159 160 161 162 163 164 165-175 176-255 Default Value 0078h 0078h 0000h 0000h 702Bh 500Ch 4000h XXXXh 001Fh 0001h 0000h 0000h 0000h 604Fh 6F00h 603Fh 0000h 0001h 0000h 81F4h 0000h 0000h 0092h 0000h 0000h 0000h Total Bytes 2 2 20 4 2 2 2 6 2 2 2 2 2 2 68 2 64 2 2 2 2 2 22 140 Data Field Type Information Minimum PIO transfer cycle time without flow control Minimum PIO transfer cycle time with IORDY flow control Reserved Reserved CF cards do not return an ATA version Command sets supported Command sets supported Command sets supported Features/command sets enabled Ultra DMA Mode Supported and Selected Time required for Security erase unit completion Time required for Enhanced security erase unit completion Current Advanced power management value Master Password Revision Code - Hardware reset result (Master) - Hardware reset result (Slave) - Hardware reset result (Master w/ slave present) Reserved Security status Vendor unique bytes Power requirement description Reserved for assignment by the CFA Key management schemes supported CF Advanced True IDE Timing Mode Capability and Setting CF Advanced PC Card I/O and Memory Timing Mode Capability Reserved Reserved Word 0: General Configuration This field indicates the general characteristics of the device. When Word 0 of the Identify drive information is 848Ah then the device is a CompactFlash Storage Card and complies with the CFA specification and CFA command set. It is recommended that PCMCIA modes of operation report only the 848Ah value as they are always intended as removable devices. Bits 15-0: CF Standard Configuration Value Word 0 is 848Ah. This is the recommended value of Word 0. Some operating systems require Bit 6 of Word 0 to be set to 1 (Non-removable device) to use the card as the root storage device. The Card must be the root storage device when a host completely replaces conventional disk storage with a CompactFlash Card in True IDE mode.

To support this requirement and provide capability for any future removable media Cards, alternatehandling of Word 0 is permitted. Bits 15-0: CF Preferred Alternate Configuration Values 044Ah: This is the alternate value of Word 0 turns on ATA device and turns off Removable Media and Transcend Information Inc. 76 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Removable Device while preserving all Retired bits in the word. 0040h: This is the alternate value of Word 0 turns on ATA device and turns off Removable Media and Removable Device while zeroing all Retired bits in the word Bit 15-12: Configuration Flag If bits 15:12 are set to 8h then Word 0 shall be 848Ah. If bits 15:12 are set to 0h then Bits 11:0 are set using the definitions below and the Card is required to support for the CFA command set and report that in bit 2 of Word 83. Bit 15:12 values other than 8h and 0h are prohibited. Bits 11-8: Retired These bits have retired ATA bit definitions. It is recommended that the value of these bits be either the preferred value of 0h or the value of 4h that preserves the corresponding bits from the 848Ah CF signature value.

Bit 7: Removable Media Device If Bit 7 is set to 1, the Card contains media that can be removed during Card operation. If Bit 7 is set to 0, the Card contains nonremovable media. Bit 6: Not Removable Controller and/or Device Alert! This bit will be considered for obsolescence in a future revision of this standard. If Bit 6 is set to 1, the Card is intended to be nonremovable during operation. If Bit 6 is set to 0, the Card is intended to be removable during operation. Bits 5-0: Retired/Reserved Alert! Bit 2 will be considered for definition in a future revision of this standard and shall be 0 at this time.

Bits 5-1 have retired ATA bit definitions. Bit 2 shall be 0. Bit 0 is Reserved and shall be 0. It is recommended that the value of bits 5-0 be either the preferred value of 00h or the value of 0Ah that preserves the corresponding bits from the 848Ah CF signature value. Word 1: Default Number of Cylinders This field contains the number of translated cylinders in the default translation mode.

This value will be the same as the number of cylinders. Word 3: Default Number of Heads This field contains the number of translated heads in the default translation mode. Word 6: Default Number of Sectors per Track This field contains the number of sectors per track in the default translation mode. Words 7-8: Number of Sectors per Card This field contains the number of sectors per CompactFlash Storage Card. This double word value is also the first invalid address in LBA translation mode. Words 10-19: Serial Number This field contains the serial number for this CompactFlash Storage Card and is right justified and padded with spaces (20h). Word 22: ECC Count This field defines the number of ECC bytes used on each sector in the Read and Write Long commands. This value shall be set to 0004h. Words 23-26: Firmware Revision This field contains the revision of the firmware for this product. Words 27-46: Model Number Transcend Information Inc.

77 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 This field contains the model number for this product and is left justified and padded with spaces (20h). Word 47: Read/Write Multiple Sector Count Bits 15-8 shall be the recommended value of 80h or the permitted value of 00h. Bits 7-0 of this word define the maximum number of sectors per block that the CompactFlash Storage Card supports for Read/Write Multiple commands. Word 49: Capabilities Bit 13: Standby Timer If bit 13 is set to 1 then the Standby timer is supported as defined by the IDLE command If bit 13 is set to 0 then the Standby timer operation is defined by the vendor. Bit 11: IORDY Supported If bit 11 is set to 1 then this CompactFlash Storage Card supports IORDY operation. If bit 11 is set to 0 then this CompactFlash Storage Card may support IORDY operation. Bit 10: IORDY may be disabled Bit 10 shall be set to 0, indicating that IORDY may not be disabled. Bit 9: LBA supported Bit 9 shall be set to 1, indicating that this CompactFlash Storage Card supports LBA mode addressing. CF devices shall support LBA addressing.

Bit 8: DMA Supported If bit 8 is set to 1 then Read DMA and Write DMA commands are supported. Bit 8 shall be set to 0. Read/Write DMA commands are not currently permitted on CF cards. PIO Data Transfer Cycle Timing Mode The PIO transfer timing for each CompactFlash Storage Card falls into modes that have unique parametric timing specifications. The value returned in Bits 15-8 shall be 00h for mode 0, 01h for mode 1, or 02h for mode 2.

Values 03h through FFh are reserved. Translation Parameters Valid Bit 0 shall be set to 1 indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors. If bit 1 of word 53 is set to 1, the values in words 64 through 70 are valid. If this bit is cleared to 0, the values reported in words 64-70 are not valid. Any CompactFlash Storage Card that supports PIO mode 3 or above shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70.

Current Number of Cylinders, Heads, Sectors/Track These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode. Current Capacity This field contains the product of the current cylinders times heads times sectors. Multiple Sector Setting Bits 15-9 are reserved and shall be set to 0. Bit 8 shall be set to 1 indicating that the Multiple Sector Setting is valid. Bits 7-0 are the current setting for the number of sectors that shall be transferred per interrupt on Read/Write Multiple commands. Total Sectors Addressable in LBA Mode This field contains the total number of user addressable sectors for the CompactFlash Storage Card in LBA mode only. Multiword DMA transfer Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Only one of bits may be set to one in this field by the CompactFlash Storage Card to indicate the multiword DMA mode which is currently selected.

Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, Transcend Information Inc. 78 V1.2 Transcend IIndustriiall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 indicates that Multiword DMA mode 0 has been selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected. Selection of Multiword DMA modes 3 and above are specific to CompactFlash are reported in word 163, Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings. Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant.

Any number of bits may be set to one in this field by the CompactFlash Storage Card to indicate the Multiword DMA modes it is capable of supporting. Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA modes 1 and 0. Bit 2, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA modes 2, 1 and 0.

Support for Multiword DMA modes 3 and above are specific to CompactFlash are reported in word 163, Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings. Word 64: Advanced PIO transfer modes supported Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the advanced PIO data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the CompactFlash Storage Card to indicate the advanced PIO modes it is capable of supporting.