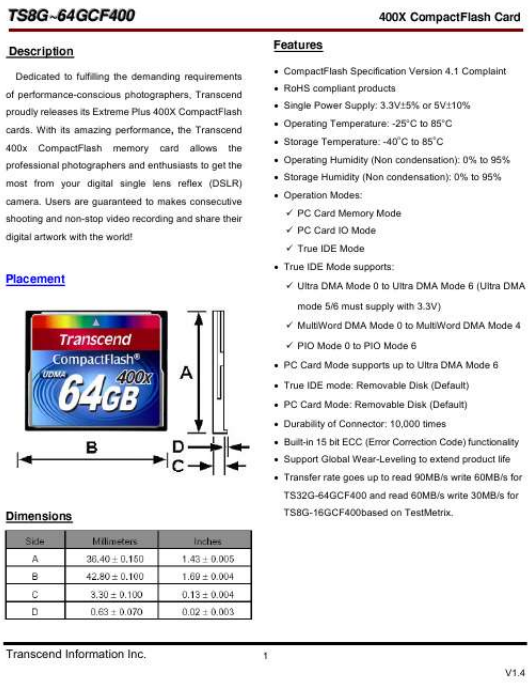

***TS8G~64GCF400*** **400X CompactFlash Card**

**Description**

Dedicated to fulfilling the demanding requirements of performance-conscious photographers, Transcend proudly releases its Extreme Plus 400X CompactFlash cards. With its amazing performance, the Transcend 400x CompactFlash memory card allows the professional photographers and enthusiasts to get the most from your digital single lens reflex (DSLR) camera. Users are guaranteed to makes consecutive shooting and non-stop video recording and share their digital artwork with the world!

**Placement**



**Dimensions**

| Side | Millimeters | Inches |
|---|---|---|
| A | 36.40 ± 0.150 | 1.43 ± 0.005 |
| B | 42.80 ± 0.100 | 1.69 ± 0.004 |
| C | 3.30 ± 0.100 | 0.13 ± 0.004 |
| D | 0.63 ± 0.070 | 0.02 ± 0.003 |

**Features**

- CompactFlash Specification Version 4.1 Complaint
- RoHS compliant products
- Single Power Supply: 3.3V±5% or 5V±10%
- Operating Temperature: -25°C to 85°C
- Storage Temperature: -40°C to 85°C
- Operating Humidity (Non condensation): 0% to 95%
- Storage Humidity (Non condensation): 0% to 95%
- Operation Modes:
  - ✓ PC Card Memory Mode
  - ✓ PC Card IO Mode
  - ✓ True IDE Mode
- True IDE Mode supports:
  - ✓ Ultra DMA Mode 0 to Ultra DMA Mode 6 (Ultra DMA mode 5/6 must supply with 3.3V)
  - ✓ MultiWord DMA Mode 0 to MultiWord DMA Mode 4
  - ✓ PIO Mode 0 to PIO Mode 6
- PC Card Mode supports up to Ultra DMA Mode 6
- True IDE mode: Removable Disk (Default)
- PC Card Mode: Removable Disk (Default)
- Durability of Connector: 10,000 times
- Built-in 15 bit ECC (Error Correction Code) functionality
- Support Global Wear-Leveling to extend product life
- Transfer rate goes up to read 90MB/s write 60MB/s for TS32G-64GCF400 and read 60MB/s write 30MB/s for TS8G-16GCF400based on TestMetrix.

***Manual abstract:***

*2) The signal should be grounded by the host. 3) The signal should be tied to VCC by the host. 4) The mode is required for CompactFlash Storage Cards. 5) The -CSEL signal is ignored by the card in PC Card modes. @@In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host. 6) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal,including a floating condition 7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active. 8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active. 9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active. 10) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Write is active. 11) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Read is active. 12) Signal usage in PC Card I/O and Memory Mode when Ultra DMA protocol is active. Transcend Information Inc. 7 V1.4 TS8G~64GCF400 TS8G~64GCF400 Input Leakage Current 400X CompactFlash Card Note: In Table 1 below, x refers to the characteristics described in table 2.*
*For example, I1U indicates a pull-up resistor with a type 1 input characteristic. Table 1: Input Leakage Current Type IxZ IxU IxD Parameter Input Leakage Current Pull-Up Resistor Pull-Down Resistor Symbol IL RPU1 RPD1 Conditions Vih = Vcc / Vil = Gnd Vcc = 5.0V Vcc = 5.0V MIN -1 50k 50k TYP MAX 1 500k 500k Units A Ohm Ohm Note: The minimum pull-up resistor resistance meets the PCMCIA PC Card specification of 10k ohms but is intentionally higher in the CompactFlash Specification to reduce power use. Input Characteristics Table 2: Input Characteristics Type Parameter Symbol MIN TYP VCC = 3. 3 V 1 2 Input Voltage CMOS Input Voltage CMOS Input Voltage CMOS Schmitt Trigger Vih Vil Vih Vil Vth Vtl 2.4 1.5 1.8 1.0 0.6 0.6 4.0 1 MAX MIN TYP VCC = 5.0 V MAX Units 0.8 0.*

*8 2.8 2.0 Volts Volts Volts 2.0 3 Notes: 1) The host provides a logic output high voltage for a CMOS load of .9 x VCC. For a 5 volt product, this translates to .9 x 4.5 = 4.05 volts minimum Voh. Output Drive Type Note: In Table 3 below, x refers to the characteristics described in Table 4.*
*For example, OT3 refers to Totem pole output with a type 3 output drive characteristic. Table 3: Output Drive Type Type OTx OZx OPx ONx Totempole Tri-State N-P Channel P-Channel Only N-Channel Only Output Type Valid Conditions Ioh & Iol Ioh & Iol Ioh Only Iol Only Transcend Information Inc. 8 V1.4 TS8G~64GCF400 TS8G~64GCF400 Output Drive Characteristics Table 4: Output Drive Characteristics Type Parameter Symbol Voh 1 Output Voltage Vol Voh 2 Output Voltage Vol Voh 3 Output Voltage Vol X Tri-State Leakage Current Ioz Iol = 4 mA Vol = Gnd Voh = Vcc -10 Iol = 4 mA Ioh = -4 mA Vcc -0.8V Iol = 4 mA Ioh = -4 mA Vcc -0.*
*8V Conditions Ioh = -4 mA MIN Vcc -0.8V 400X CompactFlash Card TYP MAX Units Gnd +0.4V Volts Gnd +0.4V Volts Gnd +0.4V 10 Volts A Transcend Information Inc.*
*9 V1.4 TS8G~64GCF400 TS8G~64GCF400 Signal Description Signal Name A10  A00 (PC Card Memory Mode) 400X CompactFlash Card Dir. I Pin Description 8,10,11,12, These address lines along with the -REG signal are used to select the following: 14,15,16,17, The I/O port address registers within the CompactFlash Storage Card , the 18,19,20 memory mapped port address registers within the CompactFlash Storage Card, a byte in the card's information structure and its configuration control and status registers. This signal is the same as the PC Card Memory Mode signal. A10  A00 (PC Card I/O Mode) A02 - A00 (True IDE Mode) I 18,19,20 In True IDE Mode, only A[02:00] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host. This signal is asserted high, as BVD1 is not supported. BVD1 (PC Card Memory Mode) I/O 46 -STSCHG (PC Card I/O Mode) Status Changed This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register. In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol. -PDIAG (True IDE Mode) BVD2 (PC Card Memory Mode) I/O 45 This signal is asserted high, as BVD2 is not supported.*

*-SPKR (PC Card I/O Mode) This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated. In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol. -DASP (True IDE Mode) -CD1, -CD2 (PC Card Memory Mode) O 26,25 These Card Detect pins are connected to ground on the CompactFlash Storage Card. They are used by the host to determine that the CompactFlash Storage Card is fully inserted into its socket. This signal is the same for all modes. -CD1, -CD2 (PC Card I/O Mode) -CD1, -CD2 (True IDE Mode) This signal is the same for all modes. Transcend Information Inc. 10 V1.4 TS8G~64GCF400 TS8G~64GCF400 400X CompactFlash Card Signal Name -CE1, -CE2 (PC Card Memory Mode) Card Enable Dir.*
*I Pin 7,32 Description These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word.-CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0,-CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Table 27, Table 29, Table 31, Table 35, Table 36 and Table 37.*
*This signal is the same as the PC Card Memory Mode modes of operation need not alter the PC Card mode connections while in True IDE mode as long as this does not prevent proper operation in any mode. -HIOE (PC Card Memory Mode except Ultra DMA Protocol Active) I 34 This signal is not used in this mode. This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card when the card is configured to use the I/O interface. In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode. In all modes when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate  HDMARDY to pause an Ultra DMA transfer. In all modes when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst. -HIOE (PC Card I/O Mode except Ultra DMA Protocol Active) -HIOE (True IDE Mode  Except Ultra DMA Protocol Active) -HDMARDY (All Modes - Ultra DMA Protocol DMA Read) HSTROBE (All Modes - Ultra DMA Protocol DMA Write) Transcend Information Inc.*

*12 V1.4 TS8G~64GCF400 TS8G~64GCF400 Signal Name -IOWR (PC Card Memory Mode Except Ultra DMA Protocol Active) 400X CompactFlash Card Pin 35 Description This signal is not used in this mode. Dir. I -IOWR (PC Card I/O Mode Except Ultra DMA Protocol Active) The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card controller registers when the CompactFlash Storage Card is configured to use the I/O interface.*

*The clocking shall occur on the negative to positive edge of the signal (trailing edge). -IOWR (True IDE Mode Except Ultra DMA Protocol Active) In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol. In All Modes, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA data burst. STOP (All Modes Ultra DMA Protocol Active) -OE (PC Card Memory Mode) I 9 This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. To enable True IDE Mode this input should be grounded by the host. -OE (PC Card I/O Mode) -ATA SEL (True IDE Mode) READY (PC Card Memory Mode) O 37 In Memory Mode, this signal is set high when the CompactFlash Storage Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card has completed its power up or reset function.*
*No access of any type should be made to the CompactFlash Storage Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state. -IREQ (PC Card I/O Mode) I/O Operation After the CompactFlash Storage Card Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.*
*In True IDE Mode signal is the active high Interrupt Request to the host. INTRQ (True IDE Mode) Transcend Information Inc. 13 V1.4 TS8G~64GCF400 TS8G~64GCF400 Signal Name -REG (PC Card Memory Mode Except Ultra DMA Protocol Active) 400X CompactFlash Card Pin 44 Description This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.*
*In PC Card Memory Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal negated during the execution of any DMA Command by the device. The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus. In PC Card I/O Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal asserted during the execution of any DMA Command by the device. This is a DMA Acknowledge signal that is asserted by the host in response to (-)DMARQ to initiate DMA transfers. In True IDE Mode, while DMA operations are not active, the card shall ignore the (-)DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PC Card and True-IDE modes of operation need not alter the PC Card mode connections while in True-IDE mode as long as this does not prevent proper operation all modes. Dir. I Attribute Memory Select -REG (PC Card I/O Mode - Except Ultra DMA Protocol Active) -DMACK (PC Card Memory Mode when Ultra DMA Protocol Active) DMACK (PC Card I/O Mode when Ultra DMA Protocol Active) -DMACK (True IDE Mode) RESET (PC Card Memory Mode) I 41 The CompactFlash Storage Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset.*

*The CompactFlash Storage Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set. RESET (PC Card I/O Mode) This signal is the same as the PC Card Memory Mode signal. -RESET (True IDE Mode) In the True IDE Mode, this input pin is the active low hardware reset from the host. VCC (PC Card Memory Mode) -- 13,38 +5 V, +3.3 V power. VCC (PC Card I/O Mode) This signal is the same for all modes. VCC (True IDE Mode) This signal is the same for all modes. Transcend Information Inc. 14 V1.4 TS8G~64GCF400 TS8G~64GCF400 Signal Name -VS1 -VS2 (PC Card Memory Mode) 400X CompactFlash Card Pin 33 40 Description Voltage Sense Signals.*
*-VS1 is grounded on the Card and sensed by the Host so that the CompactFlash Storage Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card. This signal is the same for all modes. Dir. O -VS1 -VS2 (PC Card I/O Mode) -VS1 -VS2 (True IDE Mode) This signal is the same for all modes.*
*-WAIT (PC Card Memory Mode Except Ultra DMA Protocol Active) O 42 The -WAIT signal is driven low by the CompactFlash Storage Card to signal the host to delay completion of a memory or I/O cycle that is in progress. This signal is the same as the PC Card Memory Mode signal. -WAIT (PC Card I/O Mode Except Ultra DMA Protocol Active) IORDY (True IDE Mode Except Ultra DMA Protocol Active) In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY. In all modes, when Ultra DMA mode DMA Write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive Ultra DMA data out bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer.*
*In all modes, when Ultra DMA mode DMA Read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst. -DDMARDY (All Modes Ultra DMA Write Protocol Active) DSTROBE (All Modes Ultra DMA Read Protocol Active) -WE (PC Card Memory Mode) I 36 This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card when the card is configured in the memory interface mode.*

*It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. -WE (PC Card I/O Mode) -WE (True IDE Mode) WP (PC Card Memory Mode) Write Protect -IOIS16 (PC Card I/O Mode) O 24 In True IDE Mode, this input signal is not used and should be connected to VCC by the host. Memory Mode  The CompactFlash Storage Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O Operation  When the CompactFlash Storage Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function.*

*A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle. -IOCS16 (True IDE Mode) Transcend Information Inc. 15 V1.4 TS8G~64GCF400 TS8G~64GCF400 Electrical Specification 400X CompactFlash Card The following tables indicate all D.C. Characteristics for the CompactFlash Storage Card. Unless otherwise stated, conditions are: Vcc = 5V ±10% Vcc = 3.3V ± 5% Absolute Maximum Conditions DC Characteristics CompactFlash Interface I/O at 5.0V Parameter Symbol Min.*
*Max. Unit Remark Supply Voltage High level output voltage Low level output voltage High level input voltage Low level input voltage Pull up resistance2 Pull down resistance VCC VOH VOL VIH VIL RPU RPD 4.5 VCC 0.8 4.0 2.*
*92 5.5 0.8 50 50 0.8 1.70 73 97 V V V V V V V KOhm KOhm Non-schmitt trigger 1 Schmitt trigger Non-schmitt trigger 1 Schmitt trigger CompactFlash Interface I/O at 3.*
*3V Parameter Symbol Min. Max. Unit Remark Supply Voltage High level output voltage Low level output voltage High level input voltage Low level input voltage Pull up resistance2 Pull down resistance VCC VOH VOL VIH VIL RPU RPD 3.135 VCC 0.8 2.4 2.05 3.465 0.8 52.7 47.*

*5 0.6 1.25 141 172 V V V V V V V KOhm KOhm Non-schmitt trigger 1 Schmitt trigger Non-schmitt trigger 1 Schmitt trigger 1. Include CE1, CE2, HREG, HOE, HIOE, HWE, HIOW pins 2. Include CE1, CE2, HREG, HOE, HIOE, HWE, HIOW, CSEL (P35), PDIAG, DASP pins Transcend Information Inc. 16 V1.4 TS8G~64GCF400 TS8G~64GCF400 Input Power 400X CompactFlash Card Input Characteristics for UDMA mode >4 In UDMA modes greater than 4, the following characteristics apply. Voltage output high and low values shall be met at the source connector to include the effect of series termination. Table: Input Characteristics (UDMA Mode > 4) Parameter DC supply voltage to drivers Low to high input threshold High to low input threshold Difference between input thresholds: ((V+ current value) - (V-current value)) Average of thresholds: ((V+ current value) + (V-current value))/2 Output Drive Characteristics for UDMA mode > 4 Symbol VDD3 V+ VVHYS VTHRAVG MIN 3.3 8% 1.*
*5 1.0 320 1.3 MAX Units 3.3% + 8% Volts 2.0 Volts 1.*
*5 Volts Volts 1.7 Volts In UDMA modes greater than 4, the characteristics specified in the following table apply. Voltage output high and low values shall be met at the source connector to include the effect of series termination. Table: Output Drive Characteristics (UDMA Mode > 4) Parameter Symbol MIN MAX Units DC supply voltage to drivers VDD3 3.3 8% 3.*
*3% + 8% Volts Voltage output high at -6 mA to +3 mA (at VoH2 the output shall be VoH2 VDD30.51 VDD3+0.3 Volts able to supply and sink current toVDD3) Voltage output low at 6 mA VoL2 0.51 Volts Notes: 1) IoLDASP shall be 12 mA minimum to meet legacy timing and signal integrity. 2) IoH value at 400 A is insufficient in the case of DMARQ that is pulled low by a 5.6 k resistor. 3) Voltage output high and low values shall be met at the source connector to include the effect of series termination. 4) A device shall have less than 64 A of leakage current into a 6.2 K pull-down resistor while the INTRQ signal is in the released state. Transcend Information Inc.*

*17 V1.4 TS8G~64GCF400 TS8G~64GCF400 Signal Interface 400X CompactFlash Card Electrical specifications shall be maintained to ensure data reliability. Additional requirements are necessary for Advanced Timing Modes and Ultra DMA modes operations. See next sections for additional information. Item Signal -CE1 -CE2 -REG -HIOE -IOWR -OE -WE RESET Status Signal READY -WAIT WP Card10 Pull-up to VCC 500 K R 50 K and shall be sufficient to keep inputs inactive when the pins are not connected at the host.1 Pull-up to VCC 500 K R 50 K .1,2 Pull-up to VCC 500 K R 50 K .1,2,9, Pull-up to VCC R 10 K .3 In PCMCIA PC Card modes Pull-up to VCC R 10 K .4 In True IDE mode, if DMA operation is supported by the host, Pull-down to Gnd R 5.*
*6 K .5 PC Card / True IDE hosts switch the pull-up to pull down in True IDE mode if DMA operation is supported. The PC Card mode Pull-up may be left active during True IDE mode if True IDE DMA operation is not supported. Address Data Bus Card Detect Voltage Sense Battery/Detect A[10:00] -CSEL D[15:00] -CD[2:1] -VS1 -VS2 BVD[2:1] Host10 Control Signal -INPACK 1. Connected to GND in the card Pull-up to Vcc 10 K R 100K .*
*Pull-up R 50 K .3.6 Notes: 1) Control Signals: each card shall present a load to the socket no larger than 50 pF 10 at a DC current of 700 A low state and 150 A high state, including pull-resistor. The socket shall be able to drive at least the following load 10 while meeting all AC timing requirements: (the number of sockets wired in parallel) multiplied by (50 pF with DC current 700 A low state and 150 A high state per socket). 2) Resistor is optional.*
*3) Status Signals: the socket shall present a load to the card no larger than 50 pF 10 at a DC current of 400 A low state and 100 A high state, including pull-up resistor. The card shall be able to drive at least the following load 10 while meeting all AC timing requirements: 50 pF at a DC current of 400 A low state and 100 A high state. Transcend Information Inc. 18 V1.4 TS8G~64GCF400 TS8G~64GCF400 400X CompactFlash Card 4) Status Signals: the socket shall present a load to the card no larger than 50 pF 10 at a DC current of 400 A low state and 100 A high state, including pull-up resistor. The card shall be able to drive at least the following load 10 while meeting all AC timing requirements: 50 pF at a DC current of 400 A low state and 100 A high state. 5) Status Signals: the socket shall present a load to the card no larger than 50 pF 10 at a DC current of 400 A low state and 100 A high state, including pull-up resistor. The card shall be able to drive at least the following load 10 while meeting all AC timing requirements: 50 pF at a DC current of 400 A low state and 1100 A high state. 6) BVD2 was not defined in the JEIDA 3.0 release.*

*Systems fully supporting JEIDA release 3 SRAM cards shall pull-up pin 45 (BVD2) to avoid sensing their batteries as "Low.*

*" 7) Address Signals: each card shall present a load of no more than 100pF 10 at a DC current of 450 A low state and 150 A high state. The host shall be able to drive at least the following load 10 while meeting all AC timing requirements: (the number of sockets wired in parallel) multiplied by (100pF with DC current 450 A low state and 150 A high state per socket). 8) Data Signals: the host and each card shall present a load no larger than 50pF 10 at a DC current of 450 A and 150 A high state. The host and each card shall be able to drive at least the following load 10 while meeting all AC timing requirements: 100pF with DC current 1.6mA low state and 300 A high state. This permits the host to wire two sockets in parallel without derating the card access speeds. 9) Reset Signal: This signal is pulled up to prevent the input from floating when a CFA to PCMCIA adapter is used in a PCMCIA revision 1 host. However, to minimize DC current drain through the pull-up resistor in normal operation the pull-up should be turned off once the Reset signal has been actively driven low by the host. Consequently, the input is specified as an I2Z because the resistor is not necessarily detectable in the input current leakage test.*
*10) Host and card restrictions for CF Advanced Timing Modes and Ultra DMA modes: Additional Requirements for CF Advanced Timing Modes and Ultra DMA Electrical Requirements for additional required limitations on the implementation of CF Advanced Timing modes and Ultra DMA modes respectively. Additional Requirements for CF Advanced Timing Modes The CF Advanced Timing modes include PC Card I/O and Memory modes that are 100ns or faster, PC Card Ultra DMA modes 3 or above and True IDE PIO Modes 5,6, Multiword DMA Modes 3,4 and True IDE Ultra DMA modes 3 or above. When operating in CF Advanced timing modes, the host shall conform to the following requirements: 1) Only one CF device shall be attached to the CF Bus. 2) The host shall not present a load of more than 40pF to the device for all signals, including any cabling. 3) The maximum cable length is 0.*
*15 m (6 in). The cable length is measured from the card connector to the host controller. 0.46 m (18 in) cables are not supported. 4) The -WAIT and IORDY signals shall be ignored by the host.*
*Devices supporting CF Advanced timing modes shall also support slower timing modes, to ensure operability with systems that do not support CF Advanced timing modes Transcend Information Inc. 19 V1.4 TS8G~64GCF400 TS8G~64GCF400 Ultra DMA Electrical Requirements Host and Card signal capacitance limits for Ultra DMA operation 400X CompactFlash Card The host interface signal capacitance at the host connector shall be a maximum of 25 pF for each signal as measured at 1 MHz. The card interface signal capacitance at the card connector shall be a maximum of 20 pF for each signal as measured at 1 MHz. Series termination required for Ultra DMA operation Series termination resistors are required at both the host and the card for operation in any of the Ultra DMA modes. Table describes typical values for series termination at the host and the device. Table: Typical Series Termination for Ultra DMA Signal Host Termination Device Termination -HIOE (-HDMARDY,HSTROBE) 22 ohm 82 ohm -IOWR (STOP) 22 ohm 82 ohm -CS0, -CS1 33 ohm 82 ohm A00, A01, A02 33 ohm 82 ohm -DMACK 22 ohm 82 ohm D15 through D00 33 ohm 33 ohm DMARQ 82 ohm 22 ohm INTRQ 82 ohm 22 ohm IORDY (-DDMARDY, DSTROBE) 82 ohm 22 ohm -RESET 33 ohm 82 ohm NOTE - Only those signals requiring termination are listed in this table. If a signal is not listed, series termination is not required for operation in an Ultra DMA mode. Shows signals also requiring a pull-up or pull-down resistor at the host. The actual termination values should be selected to compensate for transceiver and trace impedance to match the characteristic cable impedance.*

*Transcend Information Inc. 20 V1.4 TS8G~64GCF400 TS8G~64GCF400 400X CompactFlash Card Table: Ultra DMA Termination with Pull-up or Pull down Example Printed Circuit Board (PCB) Trace Requirements for Ultra DMA On any PCB for a host or device supporting Ultra DMA: The longest D[15:00] trace shall be no more than 0.5" longer than either STROBE trace as measured from the IC pin to the connector. The shortest D[15:00] trace shall be no more than 0.5" shorter than either STROBE trace as measured from the IC pin to the connector. Ultra DMA Mode Cabling Requirement Operation in Ultra DMA mode requires a crosstalk suppressing cable. The cable shall have a grounded line between each signal line. For True IDE mode operation using a cable with IDE (ATA) type 40 pin connectors it is recommended that the host sense the cable type using the method described in the ANSI INCITS 361-2002 AT Attachment - 6 standard, to prevent use of Ultra DMA with a 40 conductor cable. Transcend Information Inc.*
*21 V1.4 TS8G~64GCF400 TS8G~64GCF400 Attribute Memory Read Timing Specification 400X CompactFlash Card Attribute Memory access time is defined as 300 ns. Detailed timing specs are shown in Table below Speed Version Item Read Cycle Time Address Access Time Card Enable Access Time Output Enable Access Time Output Disable Time from CE Output Disable Time from OE Address Setup Time Output Enable Time from CE Output Enable Time from OE Data Valid from Address Change 300 ns Symbol tc(R) ta(A) ta(CE) ta(OE) tdis(CE) tdis(OE) tsu (A) ten(CE) ten(OE) tv(A) IEEE Symbol tAVAV tAVQV tELQV tGLQV tEHQZ tGHQZ tAVGL tELQNZ tGLQNZ tAXQX Min ns. 300 Max ns. 300 300 150 100 100 30 5 5 0 Note: All times are in nanoseconds.*
*Dout signifies data provided by the CompactFlash Storage Card to the system. The -CE signal or both the -OE signal and the -WE signal shall be de-asserted between consecutive cycle operations. Transcend Information Inc. 22 V1.4 TS8G~64GCF400 TS8G~64GCF400 400X CompactFlash Card Configuration Register (Attribute Memory) Write Timing Specification The Card Configuration write access time is defined as 250 ns.*
*Detailed timing specifications are shown in Table below. Table: Configuration Register (Attribute Memory) Write Timing Speed Version Item Write Cycle Time Write Pulse Width Address Setup Time Write Recovery Time Data Setup Time for WE Data Hold Time Symbol tc(W) tw(HWE) tsu(HA) trec(HWE) tsu(HD-HWEH) th(HD) Min ns 250 150 30 30 80 30 250 ns Max ns Note: All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card . Transcend Information Inc. 23 V1.4 TS8G~64GCF400 TS8G~64GCF400 Common Memory Read Timing Specification Cycle Time Mode: Item Output Enable Access Time Output Disable Time from HOE Address Setup Time Address Hold Time CEx Setup before HOE CEx Hold following HOE Wait Delay Falling from HOE Data Setup for Wait Release Wait Width Time2 Symbol ta(HOE) tdis(HOE) tsu(HA) th(HA) tsu(CEx) th(CEx) tv(IORDY-HOE) tv(IORDY) tw(IORDY) IEEE Symbol tGLQV tGHQZ tAVGL tGHAX tELGL tGHEH tGLWTV tQVWTH tWTLWTH 30 20 5 20 35 0 350 250 ns Min ns.*

*Max ns. 125 100 15 15 5 15 400X CompactFlash Card 120 ns Min ns. Max ns. 60 60 100 ns Min ns.*

*Max ns. 50 50 10 15 5 15 80 ns Min ns. Max ns. 45 45 10 10 5 10 35 0 350 35 0 350 na na na 1 1 1 Notes:1) WAIT is not supported in this mode. 2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA PC Card specification of 12µs but is intentionally less in this specification.*

*Transcend Information Inc. 24 V1.4 TS8G~64GCF400 TS8G~64GCF400 Common Memory Write Timing Specification Cycle Time Mode: Item Data Setup before HWE Data Hold following HWE HWE Pulse Width Address Setup Time CEx Setup before HWE Write Recovery Time Address Hold Time CEx Hold following HWE Wait Delay Falling from HWE WE High from Wait Release Wait Width Time2 Symbol tsu (HD-HWEH) th(HD) tw(HWE) tsu(HA) tsu(CEx) trec(HWE) th(HA) th(CEx) tv (IORDY-HWE) tv(IORDY) tw (IORDY) IEEE Symbol tDVWH tWMDX tWLWH tAVWL tELWL tWMAX tGHAX tGHEH tWLWTV tWTHWH tWTLWTH 0 350 250 ns Min ns. 80 30 150 30 5 30 20 20 35 0 Max ns. 400X CompactFlash Card 120 ns Min ns. 50 15 70 15 5 15 15 15 35 0 350 Max ns. 100 ns Min ns. 40 10 60 10 5 15 15 15 35 Max ns. 80 ns Min ns. 30 10 55 10 5 15 15 10 na1 na1 Max ns. 350 na1 Notes: 1) WAIT is not supported in this mode. 2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The -WAIT signal may be ignored if the -HWE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA PC Card specification of 12s but is intentionally less in this specification. Transcend Information Inc. 25 V1.4 TS8G~64GCF400 TS8G~64GCF400 I/O Input (Read) Timing Specification Cycle Time Mode: Item Data Delay after HIOE Data Hold following HIOE HIOE Width Time Address Setup before HIOE Address Hold following HIOE CEx Setup before HIOE CEx Hold following HIOE HREG Setup before HIOE HREG Hold following HIOE Wait Delay Falling from HIOE Data Delay from Wait Rising Wait Width Time 2 2 2 400X CompactFlash Card 250 ns Min ns.*

*Max ns. 100 0 165 70 20 5 20 5 0 35 0 350 5 120 ns Min ns. Max ns. 50 5 100 ns Min ns. Max ns. 50 5 80 ns Min ns. Max ns. 45 Symbol td(HIOE) th(HIOE) tw(HIOE) tsuA(HIOE) thA(HIOE) tsuCE(HIOE) thCE(HIOE) tsuREG (HIOE) thREG (HIOE) tdWT(HIOE) td(IORDY) tw(IORDY) IEEE Symbol tlGLQV tlGHQX tlGLIGH tAVIGL tlGHAX tELIGL tlGHEH tRGLIGL tlGHRGH tlGLWTL tWTHQV tWTLWTH 70 25 10 5 10 5 0 35 0 350 65 25 10 5 10 5 0 35 0 350 55 15 10 5 10 5 0 Na 1 1 1 Na Na Transcend Information Inc. 26 V1.4 TS8G~64GCF400 TS8G~64GCF400 I/O Output (Write) Timing Specification Cycle Time Mode: Item Data Setup before HIOW Data Hold following HIOW HIOW Width Time Address Setup before HIOW Address Hold following HIOW CEx Setup before HIOW CEx Hold following HIOW HREG Setup before HIOW HREG Hold following HIOW Wait Delay Falling from HIOW HIOW high from Wait high Wait Width Time 2 2 2 400X CompactFlash Card 255 ns Min ns.*

*60 30 165 70 20 5 20 5 0 35 0 350 0 Max ns. 120 ns Min ns. 20 10 70 25 20 5 20 5 0 35 0 350 Max ns. 100 ns Min ns. 20 5 65 25 10 5 10 5 0 35 Max ns. 80 ns Min ns. 15 5 55 15 10 5 10 5 0 Na Na 1 1 Symbol tsu(HIOW) th(HIOW) tw(HIOW) tsuA(HIOW) thA(HIOW) tsuCE (HIOW) thCE (HIOW) tsuREG (HIOW) thREG (HIOW) tdWT(HIOW) tdrHIOW (IORDY) tw(IORDY) IEEE Symbol tDVIWH tlWHDX tlWLIWH tAVIWL tlWHAX tELIWL tlWHEH tRGLIWL tlWHRGH tlWLWTL tWTJIWH tWTLWTH Max ns. 350 Na 1 Transcend Information Inc. 27 V1.4 TS8G~64GCF400 TS8G~64GCF400 True IDE PIO Mode Read/Write Timing Specification Item 0 t0 t1 t2 t2i t3 t4 t5 t6 T6Z t7 t8 t9 tRD tA tB tC Cycle time (min) Address Valid to HIOE/HIOW setup (min) HIOE/HIOW (min) HIOE/HIOW (min) Register (8 bit) HIOE/HIOW recovery time (min) HIOW data setup (min) HIOW data hold (min) HIOE data setup (min) HIOE data hold (min) HIOE data tristate (max) Address valid to -IOCS16 assertion (max) Address valid to -IOCS16 released (max) HIOE/HIOW to address valid hold Read Data Valid to IORDY active (min), if IORDY initially low after tA IORDY Setup time IORDY Pulse Width (max) IORDY assertion to release (max) 600 70 165 290 60 30 50 5 30 90 60 20 0 35 1250 5 1 383 50 125 290 45 20 35 5 30 50 45 15 0 35 1250 5 2 240 30 100 290 30 15 20 5 30 40 30 10 0 35 1250 5 Mode 3 180 30 80 80 70 30 10 20 5 30 n/a n/a 10 0 35 1250 5 400X CompactFlash Card Note 4 120 25 70 70 25 20 10 20 5 30 n/a n/a 10 0 35 1250 5 5 100 15 65 65 25 20 5 15 5 20 n/a n/a 10 0 na na na 5 5 5 6 80 10 55 55 20 15 5 10 5 20 n/a n/a 10 0 na na na 5 5 5 1 1 1 1 2 4 4 3 Notes: All timings are in nanoseconds.*

*The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -HIOE high is 0 nsec, but minimum -HIOE width shall still be met. 1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation. 2) This parameter specifies the time from the negation edge of -HIOE to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).*

*3) The delay from the activation of -HIOE or -HIOW until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of -HIOE or -HIOW, then t5 shall be met and tRD is not applicable. If the CompactFlash Storage Card is driving IORDY negated at the time tA after the activation of -HIOE or -HIOW, then tRD shall be met and t5 is not applicable. 4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid. 5) IORDY is not supported in this mode. Transcend Information Inc. 28 V1.4 TS8G~64GCF400 TS8G~64GCF400 400X CompactFlash Card Transcend Information Inc. 29 V1.*

*4 TS8G~64GCF400 TS8G~64GCF400 True IDE Multiword DMA Mode Read/Write Timing Specification Item tO tD tE tF tG tH tI tJ tKR tKW tLR tLW tM tN Cycle time (min) -HIOE / -HIOW asserted width (min) -HIOE data access (max) -HIOE data hold (min) -HIOE/-HIOW data setup (min) -HIOW data hold (min) -HREG to HIOE/-HIOW setup (min) -HIOE / -HIOW to -HREG hold (min) -HIOE negated width (min) -HIOW negated width (min) -HIOE to DMARQ delay (max) -HIOW to DMARQ delay (max) CEx valid to HIOE / -HIOW CEx hold Mode 0 (ns) 480 215 150 5 100 20 0 20 50 215 120 40 50 15 Mode 1 (ns) 150 80 60 5 30 15 0 5 50 50 40 40 30 10 Mode 2 (ns) 120 70 50 5 20 10 0 5 25 25 35 35 25 10 400X CompactFlash Card Mode 3 (ns) 100 65 50 5 15 5 0 5 25 25 35 35 10 10 Mode 4 (ns) 80 55 45 5 10 5 0 5 20 20 35 35 5 10 Note 1 1 1 1 Transcend Information Inc. 30 V1.4 TS8G~64GCF400 TS8G~64GCF400 400X CompactFlash Card True IDE Ultra DMA Mode Read/Write Timing Specification Ultra DMA operations can take place in any of the three basic interface modes: PC Card Memory mode, PC Card I/O mode, Transcend Information Inc. 31 V1.*
*4 TS8G~64GCF400 TS8G~64GCF400 400X CompactFlash Card and True IDE (the original mode to support UDMA). The usage of signals in each of the modes is shown in Table 24:Ultra DMA Signal Usage In Each Interface Mode Pin # (Non PC CARD MEM PC CARD IO MODE TRUE IDE MODE UDMA Signal Type UDMA MEM MODE UDMA UDMA UDMA MODE) DMARQ HREG HIOW HIOE Output Input Input Input 43 (-INPACK) 44 (-REG) 35 (-HIOW) 34 (-HIOE) -DMARQ -DMACK STOP 1 -HDMARDY(R) , 1, 3, 4 2HSTROBE(W) -DDMARDY(W) DSTROBE(R) 1. 2. 4 D[15:00] A[10:00] -CSEL READY -CE1 -CE2 1, 3 1 -DMARQ DMACK STOP 1 -HDMARDY(R) 1, 3, 4 HSTROBE(W) -DDMARDY(W) DSTROBE(R) 1. 2.*
*4 D[15:00] A[10:00] -CSEL -INTRQ -CE1 -CE2 1, 3 1, 2 DMARQ -DMACK STOP 1 -HDMARDY(R) 1, 3, 4 HSTROBE(W) -DDMARDY(W) DSTROBE(R) 1. 2. 4 D[15:00] A[02:00] 5 -CSEL INTRQ -CS0 -CS1 1, 3 1, 2 IORDY HD [15:0] HA [10:0] CSEL HIRQ CE1 CE2 Output Bidir Input Input Output Input 42 (-WAIT) ... (D[15:00]) ... (A[10:00]) 39 (-CSEL) 37 (READY) 7 (-CE1) 31 (-CE2) Notes:1) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst. 2) The UDMA interpretation of this signal is valid only during and Ultra DMA data burst during a DMA Read command.*

*3) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command. 4) The HSTROBE and DSTROBE signals are active on both the rising and the falling edge. 5) Address lines 03 through 10 are not used in True IDE mode. Several signal lines are redefined to provide different functions during an Ultra DMA data burst. These lines assume their UDMA definitions when: 1 2 3 4 an Ultra DMA mode is selected, and a host issues a READ DMA, or a WRITE DMA command requiring data transfer, and the device asserts (-)DMARQ, and the host asserts (-)DMACK. These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of -DMACK by the host at the termination of an Ultra DMA data burst. With the Ultra DMA protocol, the STROBE signal that latches data from D[15:00] is generated by the same agent (either host or device) that drives the data onto the bus. Ownership of D[15:00] and this data strobe signal are given either to the device during an Ultra DMA data-in burst or to the host for an Ultra DMA data-out burst. During an Ultra DMA data burst a sender shall always drive data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the same frequency as the data.*
*Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to select the Ultra DMA mode at which the system operates. The Ultra DMA mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only one Ultra DMA mode shall be selected at any given time. All timing requirements for a selected Ultra DMA mode shall be satisfied.*
*Devices supporting any Ultra DMA mode shall also support all slower Ultra DMA modes. Transcend Information Inc. 32 V1.4 TS8G~64GCF400 TS8G~64GCF400 400X CompactFlash Card An Ultra DMA capable device shall retain the previously selected Ultra DMA mode after executing a software reset sequence or the sequence caused by receipt of a DEVICE RESET command if a SET FEATURES disable reverting to defaults command has been issued. The device may revert to a Multiword DMA mode if a SET FEATURES enable reverting to default has been issued.*
*An Ultra DMA capable device shall clear any previously selected Ultra DMA mode and revert to the default non-Ultra DMA modes after executing a power-on or hardware reset. Both the host and device perform a CRC function during an Ultra DMA data burst. At the end of an Ultra DMA data burst the host sends its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match, the device reports an error in the error register. If an error occurs during one or more Ultra DMA data bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error. NOTE -If a data transfer is terminated before completion, the assertion of INTRQ should be passed through to the host software driver regardless of whether all data requested by the command has been transferred. Transcend Information Inc. 33 V1.*

*4 TS8G~64GCF400 TS8G~64GCF400 Name UDMA Mode 0 Min Max UDMA Mode 1 Min 160 73 153 10.0 5.0 48.0 6.2 10.0 5.0 48.0 6.2 0 48.0 230 0 20 0 10 20 0 20 70 75 160 20 0 20 50 0 20 50 125 20 0 20 50 20 0 20 70 70 100 20 0 20 50 150 0 20 0 10 20 0 20 70 60 100 20 0 20 50 200 150 0 20 0 10 20 0 20 55 60 100 20 0 20 50 Max UDMA Mode 2 Min 120 54 115 7.*
*0 5.0 31.0 6.2 7.0 5.*
*0 31.0 6.2 0 31.0 170 150 0 20 0 10 20 0 20 55 60 85 Max UDMA Mode 3 Min 90 39 86 7.0 5.*
*0 20.0 6.2 7.0 5.0 20.0 6.2 0 20.0 130 100 0 20 0 10 20 0 20 Max UDMA Mode 4 Min 60 25 57 5.0 5.0 6.*

*7 6.2 5.0 5.0 6.7 6.2 0 6.7 120 100 0 20 0 Max 400X CompactFlash Card UDMA Mode 5 Min 40 16.8 38 4.0 4.6 4.*
*8 4.8 5.0 5.0 10.0 10.*
*0 35 25 90 75 0 20 0 10 20 0 50 50 85 20 0 20 50 20 20 50 50 10 Max UDMA Mode 6 Min 30 13.0 29 2.6 3.5 4.0 4.*
*0 5.0 5.0 10.0 10.0 25 17.5 80 60 Max Sender Note 3 Sender Recipient Recipient Sender Sender Device Device Host Host Device Sender Device Note 4 Host Host Note 5 Host Device Host Sender Recipient Device Device Host Sender Measure location (see Note 2) t2CYCTYP tCYC t2CYC tDS tDH tDVS tDVH tCS tCH tCVS tCVH tZFS tDZFS tFS tLI tMLI tUI tAZ tZAH tZAD tENV tRFS tRP tIORDYZ tZIORDY tACK tSS Notes: 240 112 230 15.*

*0 5.0 70.0 6.2 15.*

*0 5.0 70.0 6.2 0 70.0 1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V. 2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and DMARDY transitions are measured at the sender connector. 3) The parameter tCYC shall be measured at the recipient's connector farthest from the sender. 4) The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming Transcend Information Inc.*
*34 V1.4 TS8G~64GCF400 TS8G~64GCF400 400X CompactFlash Card transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector. 5) The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus the allow for a bus turnaround. Name t2CYCTYP tCYC t2CYC tDS tDH tDVS tDVH tCS tCH tCVS tCVH tZFS tDZFS tFS tLI tMLI tUI tAZ tZAH tZAD tENV tRFS tRP tIORDYZ tZIORDY tACK tSS Comment Typical sustained average two cycle time Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge) Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE) Data setup time at recipient (from data valid until STROBE edge) Data hold time at recipient (from STROBE edge until data may become invalid) Data valid setup time at sender (from data valid until STROBE edge) Data valid hold time at sender (from STROBE edge until data may become invalid) CRC word setup time at device CRC word hold time device CRC word valid setup time at host (from CRC valid until -DMACK negation) CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid) Time from STROBE output released-to-driving until the first transition of critical timing.*
*Time from data output released-to-driving until the first transition of critical timing. First STROBE time (for device to first negate DSTROBE from STOP during a data in burst) Limited interlock time Interlock time with minimum Unlimited interlock time Maximum time allowed for output drivers to release (from asserted or negated) Minimum delay time required for output drivers to assert or negate (from released) Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation) Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY) Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY) Maximum time before releasing IORDY Minimum time before driving IORDY Setup and hold times for -DMACK (before assertion or negation) Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst) 6 4, 6 1 1 1 2, 5 2, 5 3 3 2 2 3 3 Notes Transcend Information Inc. 35 V1.4 TS8G~64GCF400 TS8G~64GCF400 400X CompactFlash Card Notes: 1) The parameters tUI, tMLI : (Ultra DMA Data-In Burst Device Termination Timing and Ultra DMA Data-In Burst Host Termination Timing), and tLI indicate sender-to-recipient or recipient-to-sender interlocks, i.e.*
*, one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. tUI is an unlimited interlock that has no maximum time value. tMLI is a limited time-out that has a defined minimum. tLI is a limited time-out that has a defined maximum. 2) 80-conductor cabling shall be required in order to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes greater than 2. 3) Timing for tDVS, tDVH, tCVS and tCVH shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system. 4)For all modes the parameter tZIORDY may be greater than tENV due to the fact that the host has a pull-up on IORDY- giving it a known state when released. 5)The parameters tDS, and tDH for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for tDS and tDH for mode 5 at the middle connector being 3.*

*0 and 3.9 ns respectively. Name UDMA Mode 0 (ns) Min Max UDMA Mode 1 (ns) Min 9.7 4.8 50.9 9.0 Max UDMA Mode 2 (ns) Min 6.8 4.8 33.9 9.*
*0 Max UDMA Mode 3 (ns) Min 6.8 4.8 22.6 9.0 Max UDMA Mode4 (ns) Min 4.*
*8 4.8 9.5 9.0 Max UDMA Mode 5 (ns) Min 2.3 2.*
*8 6.0 6.0 Max UDMA Mode 6 (ns) Min 2.3 2.8 5.2 5.2 Max tDSIC tDHIC tDVSIC tDVHIC tDSIC tDHIC tDVSIC tDVHIC 14.7 4.8 72.9 9.*

*0 Recipient IC data setup time (from data valid until STROBE edge) (see note 2) Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2) Sender IC data valid setup time (from data valid until STROBE edge) (see note 3) Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3) Notes: 1) All timing measurement switching points(low to high and high to low) shall be taken at 1.5 V. 2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V). 3)The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values. Transcend Information Inc. 36 V1.*
*4 TS8G~64GCF400 TS8G~64GCF400 Name Comment 400X CompactFlash Card Min [V/ns] Max [V/ns] Notes SRISE SFALL Rising Edge Slew Rate for any signal Falling Edge Slew Rate for any signal 1.25 1.25 1 1 Note: 1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient.*
*The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector. The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.*
*05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values. Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope.*

*The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge. Transcend Information Inc. 37 V1.4 TS8G~64GCF400 TS8G~64GCF400 Card Configuration 400X CompactFlash Card The CompactFlash Storage Cards is identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the CompactFlash Storage Card that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.*

*Multiple Function CompactFlash Storage Cards ! Table: CompactFlash Storage Card Registers and Memory Space Decoding -CE2 1 X 1 0 0 X 1 0 0 X 1 1 1 0 0 -CE1 1 0 0 1 0 0 0 1 0 0 0 0 0 1 1 -REG X 0 1 1 1 0 1 1 1 0 0 0 0 0 0 -OE X 0 0 0 0 1 1 1 1 0 1 0 1 0 1 -WE X 1 1 1 1 0 0 0 0 1 0 1 0 1 0 A10 X 0 X X X 0 X X X 0 0 X X X X A9 X 1 X X X 1 X X X 0 0 X X X X A8-A4 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX A3 X X X X X X X X X X X X X X X A2 X X X X X X X X X X X X X X A1 X X X X X X X X X X X X X X A0 X 0 X X 0 0 X X 0 0 0 1 1 X X SELECTED SPACE Standby and UDMA transfer Configuration Registers Read Common Memory Read (8 Bit D7-D0) Common Memory Read (8 Bit D15-D8) Common Memory Read (16 Bit D15-D0) Configuration Registers Write Common Memory Write (8 Bit D7-D0) Common Memory Write (8 Bit D15-D8) Common Memory Write (16 Bit D15-D0) Card Information Structure Read Invalid Access (CIS Write) Invalid Access (Odd Attribute Read) Invalid Access (Odd Attribute Write) Invalid Access (Odd Attribute Read) Invalid Access (Odd Attribute Write) Transcend Information Inc. 38 V1.4 TS8G~64GCF400 TS8G~64GCF400 -DMARQ -INPACK 1 0 0 0 0 0 0 0 0 0 0 1 1 0 1 1 1 1 -DMACK -REG X 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 / 1 STOP -HIO W X X 1 1 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 -DMARDY -HIOE (R)-WAIT (W) X X X 1 1 0 X 1 0 1 0 0 1 0 1 1 1 1 STROBE -WAIT (R)-HIOE (W) X 1 1 1 1 1 / or \ 0 or 1 0 or 1 0 or 1 0 or 1 0 or 1 0 or 1 0 or 1 / 1 1 DMA CMD No YES YES YES YES YES YES RD RD WR WR RD RD YES YES YES YES YES A10A00 XX XX XX Static Static Static Static Static Static Static Static Static Static Static Static Static Static 400X CompactFlash Card Table: PC Card Memory Mode UDMA Function -CE2 1 X X 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 -CE1 1 X X 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 Operation Standby Device UDMA Transfer Request (Assert DMARQ) Host Acknowledge Preparation Host Acknowledge Preparation DMA Acknowledge (Stopped) Burst Initiation / Active Burst Transfer Data In Burst Host Pause Data In Burst Device Pause Data Out Burst Device Pause Data Out Burst Host Pause Device Initiating BurstTermination Host Acknowledement of Device Initiated Burst Termination Host Initiating BurstTermination Device Acknowledging Host Initiated Burst Termination Device Aligning STROBE to Asserted before CRC Transfer CRC Data Transfer for UDMA Burst Burst Completed Table: CompactFlash Storage Card Configuration Registers Decoding -CE2 X X X X X X X -CE1 0 0 0 0 0 0 0 0 -REG 0 0 0 0 0 0 0 0 -OE 0 1 0 1 0 1 0 1 -WE 1 0 1 0 1 0 1 0 A10 0 0 0 0 0 0 0 0 A9 1 1 1 1 1 1 1 1 A8-A4 00 00 00 00 00 00 00 00 A3 0 0 0 0 0 0 0 0 A2 0 0 0 0 1 1 1 1 A1 0 0 1 1 0 0 1 1 A0 0 0 0 0 0 0 0 0 SELECTED REGISTER Configuration Option Reg Read Configuration Option Reg Write Card Status Register Read Card Status Register Write Pin Replacement Register Read Pin Replacement Register Write Socket and Copy Register Read Socket and Copy Register Write Transcend Information Inc. 39 V1.4 TS8G~64GCF400 TS8G~64GCF400 Attribute Memory Function 400X CompactFlash Card Attribute memory is a space where CompactFlash Storage Card identification and configuration information are stored, and is limited to 8 bit wide accesses only at even addresses. The card configuration registers are also located here. For CompactFlash Storage Cards, the base address of the Card configuration registers is 200h. Table: Attribute Memory Function Function Mode Standby Mode Standby Mode UDMA Operation (see section 4.3.18: Ultra DMA Mode Read/Write Timing Specification) Read Byte Access CIS ROM (8 bits) Write Byte Access CIS (8 bits) (Invalid) Read Byte Access Configuration CompactFlash Storage (8 bits) Write Byte Access Configuration CompactFlash Storage (8 bits) Read Word Access CIS (16 bits) Write Word Access CIS (16 bits) (Invalid) Read Word Access Configuration CompactFlash Storage (16 bits) Write Word Access Configuration CompactFlash Storage (16 bits) DMA CMD Don't Care No Yes -REG H X L1 -CE2 H H H -CE1 H H H A10 X X X A9 X X X A0 X X X -OE X X H -WE X X H D15-D8 High Z High Z Odd Byte D7-D0 High Z High Z Even Byte Even Byte Even Byte Even Byte Even Byte Even Byte Even Byte Even Byte Even Byte No No No L L L H H H L2 L2 L L L L L L H L L L L2 H L H L2 H High Z Don't Care High Z Don't Care Not Valid Don't Care Not Valid Don't Care No No No No L L L L H L2 L2 L2 L L2 L2 L2 L L L L H L L H L X X X H L2 H L2 L H L2 H No L L2 L2 L H X H L2 Notes: 1) In UDMA operation, the -REG (-DMACK) signal shall be asserted only in response to -DMARQ. 2) The -CE signals or both the -OE signal and the -WE signal shall be de-asserted between consecutive cycle operations. Transcend Information Inc. 40 V1.4 TS8G~64GCF400 TS8G~64GCF400 400X CompactFlash Card Configuration Option Register (Base + 00h in Attribute Memory) Transcend Information Inc. 41 V1.*

*4 TS8G~64GCF400 TS8G~64GCF400 400X CompactFlash Card Card Configuration and Status Register (Base + 02h in Attribute Memory) Transcend Information Inc. 42 V1.4 TS8G~64GCF400 TS8G~64GCF400 Pin Replacement Register (Base + 04h in Attribute Memory) 400X CompactFlash Card Transcend Information Inc. 43 V1.4 TS8G~64GCF400 TS8G~64GCF400 Socket and Copy Register (Base + 06h in Attribute Memory) 400X CompactFlash Card Transcend Information Inc.*

*44 V1.4 TS8G~64GCF400 TS8G~64GCF400 I/O Transfer Function 400X CompactFlash Card The I/O transfer to or from the CompactFlash Storage can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash Storage. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash Storage, the system shall generate a pair of 8 bit references to access the word`s even byte and odd byte. The CompactFlash Storage Card permits both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash Storage responds.*

*The CompactFlash Storage Card may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle. Table: PCMCIA Mode I/O Function Function Code Standby Mode UDMA Write UDMA Read Byte Input Access (8 bits) Byte Output Access (8 bits) Word Input Access (16 bits) Word Output Access (16 bits) I/O Read Inhibit I/O Write Inhibit High Byte Input Only (8 bits) High Byte Output Only (8 bits) DMA CMD No Write Read X X X X X X X X -REG X H H L L L L L L H H L L -CE2 H H H H H H H L L X X L L -CE1 H H H L L L L L L X X H H A0 X X X L H L H L L X X X X -HIOE X X X L L H H L H L H L H -HIOW X X X H H L L H L H L H L D15-D8 High Z Odd Byte Odd Byte High Z High Z Don't Care Don't Care Odd-Byte Odd-Byte Don't Care High Z Odd-Byte Odd-Byte D7-D0 High Z Even Byte Even Byte Even-Byte Odd-Byte Even-Byte Odd-Byte Even-Byte Even-Byte Don't Care High Z High Z Don't Care Transcend Information Inc. 45 V1.4 TS8G~64GCF400 TS8G~64GCF400 -DMARDY -HIOE (R)-WAIT (W) X X X 1 1 0 X 1 0 1 0 0 1 0 1 1 1 1 STROBE -WAIT (R)-HIOE (W) X 1 1 1 1 1 / or \ 0 or 1 0 or 1 0 or 1 0 or 1 0 or 1 0 or 1 0 or 1 0 or 1 / 1 1 400X CompactFlash Card Table: PC Card I/O Mode UDMA Function -CE2 1 X X 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 -CE1 1 X X 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 -DMARQ -INPACK 1 0 0 0 0 0 0 0 0 0 0 0 1 1 0 1 1 1 1 DMACK -REG X 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 \ 0 STOP -HIOW X X 1 1 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 DMA CMD No YES YES YES YES YES YES RD RD WR WR RD RD YES YES YES YES YES A10A00 XX XX XX Static Static Static Static Static Static Static Static Static Static Static Static Static Static Static Static Standby Operation Device UDMA Transfer Request (Assert DMARQ) Host Acknowledge Preparation Host Acknowledge Preparation DMA Acknowledge (Stopped) Burst Initiation / Active Burst Transfer Data In Burst Host Pause Data In Burst Device Pause Data Out Burst Device Pause Data Out Burst Host Pause Device Initiating BurstTermination Host Acknowledement of Device Initiated Burst Termination Host Initiating BurstTermination Device Acknowledging Host Initiated Burst Termination Device Aligning STROBE to Asserted before CRC Transfer CRC Data Transfer for UDMA Burst Burst Completed Transcend Information Inc.*

*46 V1.4 TS8G~64GCF400 TS8G~64GCF400 Common Memory Transfer Function 400X CompactFlash Card The Common Memory transfer to or from the CompactFlash Storage can be either 8 or 16 bits. Table: Common Memory Function Function Code Standby Mode Byte Read (8 bits) Byte Write (8 bits) Word Read (16 bits) Word Write (16 bits) DMA None Don't Care Don't Care Don't Care Don't Care Don't Care Write Read -REG X H H H H H H -CE2 H H H H H L L -CE1 H L L L L L L A0 X L H L H X X -OE X L L H H L H -WE X H H L L H L D15-D8 High Z High Z High Z Don't Care Don't Care Odd-Byte Odd-Byte D7-D0 High Z Even-Byte Odd-Byte Even-Byte Odd-Byte Even-Byte Even-Byte Odd Byte Read Only (8 bits) H L H X L H Odd-Byte High Z Odd Byte Write Only (8 bits) Ultra DMA Write Ultra DMA Read H L L L H H H H H X X X H H H L H H Odd-Byte Odd-Byte Odd-Byte Don't Care Even-Byte Even-Byte Transcend Information Inc. 47 V1.4 TS8G~64GCF400 TS8G~64GCF400 True IDE Mode I/O Transfer Function 400X CompactFlash Card The CompactFlash Storage Card can be configured in a True IDE Mode of operation. The CompactFlash Storage Card is configured in this mode only when the -OE input signal is grounded by the host during the power off to power on cycle. Optionally, CompactFlash Storage Cards may support the following optional detection methods: 1. The card is permitted to monitor the OE (-ATA SEL) signal at any time(s) and switch to PCMCIA mode upon detecting a high level on the pin. 2. The card is permitted to re-arbitrate the interface mode determination following a transition of the (-)RESET pin. 3. The card is permitted to monitor the OE (-ATA SEL) signal at any time(s) and switch to True IDE mode upon detection of a continuous low level on pin for an extended period of time. Table: True IDE Mode I/O Function defines the function of the operations for the True IDE Mode. Transcend Information Inc. 48 V1.*

*4 TS8G~64GCF400 TS8G~64GCF400 400X CompactFlash Card Host Configuration Requirements for Master/Slave or New Timing Modes The CF Advanced Timing modes include PCMCIA PC Card style I/O modes that are faster than the original 250 ns cycle time. These modes are not supported by the PCMCIA PC Card specification nor CF by cards based on revisions of the CF specification before Revision 3.0. Hosts shall ensure that all cards accessed through a common electrical interface are capable of operation at the desired, faster than 250 ns, I/O mode before configuring the interface for that I/O mode. Advanced Timing modes are PCMCIA PC Card style I/O modes that are 100 ns or faster, PC Card Memory modes that are 100ns or faster, True IDE PIO Modes 5,6 and Multiword DMA Modes 3,4.*

*These modes are permitted to be used only when a single card is present and the host and card are connected directly, without a cable exceeding 0.15m in length. Consequently, the host shall not configure a card into an Advanced Timing Mode if two cards are sharing I/O lines, as in Master/Slave operation, nor if it is constructed such that a cable exceeding 0.15 meters is required to connect the host to the card. The load presented to the Host by cards supporting Ultra DMA is more controlled than that presented by other CompactFlash cards. Therefore, the use of a card that does not support Ultra DMA in a Master/Slave arrangement with a Ultra DMA card can affect the critical timing of the Ultra DMA transfers. The host shall not configure a card into Ultra DMA mode when a card not supporting Ultra DMA is also present on the same interface When the use of two cards on an interface is otherwise permitted, the host may use any mode that is supported by both cards, but to achieve maximum performance it should use its highest performance mode that is also supported by both cards. Metaformat Overview The goal of the Metaformat is to describe the requirements and capabilities of the CompactFlash Storage Card as thoroughly as possible. This includes describing the power requirements, IO requirements, memory requirements, manufacturer information and details about the services provided. Table: Sample Device Info Tuple Information for Extended Speeds Note: The value "1" defined for D3 of the N+0 words indicates that no write-protect switch controls writing the ATA registers.*

*The value "0" defined for D7 in the N+2 words indicates that there is not more than a single speed extension byte. Transcend Information Inc. 49 V1.4 TS8G~64GCF400 TS8G~64GCF400 CF-ATA Drive Register Set Definition and Protocol 400X CompactFlash Card The CompactFlash Storage Card can be configured as a high performance I/O device through: a) The standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary) or 170h- 177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ).*