Your PDF Guides

You can read the recommendations in the user guide, the technical guide or the installation guide for TRANSCEND TS16GMSA300. You'll find the answers to all your questions on the TRANSCEND TS16GMSA300 in the user manual (information, specifications, safety advice, size, accessories, etc.). Detailed instructions for use are in the User's Guide.

User manual TRANSCEND TS16GMSA300
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TS2G~16GMSA500
TS16G~64GMSA300

Transcend
mSATA SSD

Description

The Transcend TSxGMSA500/TSxGMSA300 is a series of mSATA SSD device with high performance and quality Flash Memory assembled on a printed circuit board. These devices feature cutting-edge technique to enhance product life and data retention. By using these techniques, the product is designed especially for some tough applications, like industrial PC, vehicle PC and road surveillance record.

Placement
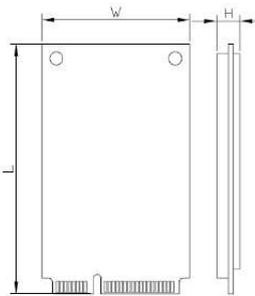
Features

- RoHS compliant
- Power Supply: 3.3V±5%
- Operating Temperature: 0°C to 70°C
- Storage Temperature: -40°C to 85°C
- Humidity (Non condensation): 0% to 95%
- TSxGMSA500 Built-in 8-bit/512Byte ECC (Error Correction Code) functionality ensures highly reliable of data transfer.
- TSxGMSA300 Built-in 15-bit/512Byte ECC (Error Correction Code) functionality ensures highly reliable of data transfer.
- Global wear-leveling algorithm eliminates excessive write operation and extends product life.
- Support StaticDataRefresh & EarlyRetirement technology to monitor error bit level and react before data is corrupted.
- Support S.M.A.R.T (Self-defined)
- Support Security Command
- Fully compatible with devices and OS that support the SATA 3Gb/s standard
- Non-volatile SLC/MLC Flash Memory for outstanding data retention

Dimensions

Side	Millimeters	Inches
W	29.85	1.175
L	50.80	2.000
H	3.5	0.137

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V1.3

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http://yourpdfguides.com/dref/3809904

Manual abstract:

These devices feature cutting-edge technique to enhance product life and data retention. By using these techniques, the product is designed especially for some tough applications, like industrial PC, vehicle PC and road surveillance record. ·mSATA SSD Features · · · · · · RoHS compliant Power Supply: 3.3V±5% Operating Temperature: 0oC to 70oC Storage Temperature: -40oC to 85oC Humidity (Non condensation): 0% to 95% TSxGMSA500 Built-in 8-bit/512Byte ECC (Error Correction Code) functionality ensures highly reliable of data transfer. TSxGMSA300 Built-in 15-bit/512Byte ECC (Error Correction Code) functionality ensures highly reliable of Placement · data transfer. Global wear-leveling algorithm eliminates excessive write operation and extends product life. · Support StaticDataRefresh & EarlyRetirement technology to monitor error bit level and react before data is corrupted. · · ·Support S.M.A.

R.T (Self-defined) Support Security Command Fully compatible with devices and OS that support the SATA 3Gb/s standard Non-volatile SLC/MLC Flash Memory for outstanding data retention · Dimensions Side W L H Millimeters 29.85 50.80 3.5 Inches 1.

175 2.000 0.137 Transcend Information Inc. 1 V1.3 TS2G~16GMSA500 TS16G~64GMSA300 Specifications Physical Specification Form Factor Storage Capacities Length Dimensions (mm) Width Height Input Voltage Weight Connector MO-300 2GB~64GB 50.

8 ± 0.15 29.85 ± 0.15 3.5 ± 0.1 3.3V ± 5% 9g PCI Express Mini Card Connector mSATA SSD Environmental Specifications Operating Temperature Storage Temperature Humidity Operating Non-Operating 0 to 70 -40 to 85 0% to 95% (Non-condensing) 0% to 95% (Non-condensing) Regulations Compliance CE, FCC and BSMI Performance Model P/N TS2GMSA500 TS4GMSA500 TS8GMSA500 TS16GMSA500 Read 50 MB/s 50 MB/s 100 MB/s 100 MB/s Write 25 MB/s 45 MB/s 80 MB/s 90 MB/s Random Read 50 MB/s 50 MB/s 80 MB/s 80 MB/s Random Write 8 MB/s 12 MB/s 15 MB/s 15 MB/s Performance Model P/N TS16GMSA300 TS32GMSA300 TS64GMSA300 Read 95 MB/s 95 MB/s 95 MB/s Write 15 MB/s 20 MB/s 30 MB/s 2 V1.3 Random Read 55 MB/s 70 MB/s 55 MB/s Random Write 5 MB/s 5 MB/s 9 MB/s Transcend Information Inc. TS2G~16GMSA500 TS16G~64GMSA300 ® mSATA SSD Note:25 , Typical value, test on ASUS P4S800-MX, 1GB RAM, Windows XP Version 2002 SP2, benchmark utility HDBENCH (version 3.4006), copied file 1GB Actual Capacity Model P/N TS2GMSA500 TS4GMSA500 TS8GMSA500 TS16GMSA500 TS16GMSA300 TS32GMSA300 TS64GMSA300 User Max.

LBA 3,865,680 7,732,368 15,465,344 30,932,992 30,932,992 61,865,984 123,731,968 Cylinder 3,835 7,671 15,343 16,383 16,383 16.383 16,383 Head 16 16 16 15 15 15 15 Sector 63 63 63 63 63 63 63 Power Requirements Input Voltage Mode Write(peak) Power Consumption Read(peak) Idle(peak) 3.3V ± 5% Max. (mA) 352 371 141 SHOCK & Vibration Test Condition Mechanical Shock Test Vibration Test 1500G, 0.5ms, 3 axes 20G (Peak-to-Peak) 20Hz to 2000Hz (Frequency) Standard IEC 60068-2-27 IEC 60068-2-6 Transcend Information Inc. 3 V1.3 TS2G~16GMSA500 TS16G~64GMSA300 Package Dimensions mSATA SSD Below figure illustrates the Transcend mSATA Solid State Disk product. All dimensions are in mm. Transcend Information Inc. 4 V1. 3 TS2G~16GMSA500 TS16G~64GMSA300 Pin Assignments Pin No. @@@@@@This is known as dynamic wear leveling. @@ECC algorithm Using 15bit BCH Error Correction Code with each channel, the controller can correct 15 random bits per 512 byte data sector for MLC NAND flash. The hardware executes parity generation and error detection/correction features. StaticDataRefresh Technology Normally, ECC engine corrections are taken place without affecting the host normal operations.

As time passes by, the number of error bits accumulated in the read transaction exceeds the correcting capability of the ECC engine, resulting in corrupted data being sent to the host. To prevent this, the controller monitors the error bit levels at each read operation; when it reaches the preset threshold value, the controller automatically performs data refresh to "restore" the correct charge levels in the cell. This implementation practically restores the data to its original, error-free state, and hence, lengthening the life of the data. EarlyRetirement Technology The StaticDataRefresh feature functions well when the cells in a block are still healthy. As the block ages over time, it cannot reliably store charge anymore and EarlyRetirement enters the scene.

EarlyRetirement works by moving the static data to another block (a health block) before the previously used block becomes completely incapable of holding charges for data. When the charge loss error level exceeds another threshold value (higher from that for StaticDataRefresh), the controller automatically moves its data to another block. In addition, the original block is then marked as a bad block, which prevents its further use, and thus the block enters the state of "EarlyRetirement." Note that, through this process, the incorrect data are detected and effectively corrected by the ECC engine, thus the data in the new block is stored error-free. Transcend Information Inc. 7 V1.3 TS2G~16GMSA500 TS16G~64GMSA300 mSATA Interface Out of bank signaling mSATA SSD There shall be three Out Of Band (OOB) signals used/detected by the Phy: COMRESET, COMINIT, and COMWAKE. COMINIT, COMRESET and COMWAKE OOB signaling shall be achieved by transmission of either a burst of four Gen1 ALIGNP primitives or a burst composed of four Gen1 Dwords with each Dword composed of four D24.3 characters, each burst having a duration of 160 UIOOB. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in Figure 4 and Table 2.

Figure 4: OOB signals Table 2: OOB signal times Transcend Information Inc. 8 V1.3 TS2G~16GMSA500 TS16G~64GMSA300 COMRESET mSATA SSD COMRESET always originates from the host controller, and forces a hardware reset in the device. It is indicated that transmitting bursts of data separated by an idle bus condition. The OOB COMRESET signal shall consist of no less than six data bursts, including inter-burst temporal spacing. The COMRESET signal shall be: 1) Sustained/continued uninterrupted as long as the system hard reset is asserted, or 2) Started during the system hardware reset and ended some time after the negation of system hardware reset, or 3) Transmitted immediately following the negation of the system hardware reset signal. The host controller shall ignore any signal received from the device from the assertion of the hardware-reset signal until the COMRESET signal is transmitted. Each burst shall be 160 Gen1 UI's long (106.7 ns) and each inter-burst idle state shall be 480 Gen1 UI's long (320 ns). A COMRESET detector looks for four consecutive bursts with 320 ns spacing (nominal).

Any spacing less than 175 ns or greater than 525 ns, it shall invalidate the COMRESET detector output. The COMRESET interface signal to the Phy layer shall initiate the Reset sequence shown in Figure 5 below. The interface shall be held inactive for at least 525 ns after the last burst to ensure far-end detector detects the negation properly. Figure 5: Comreset sequence Transcend Information Inc. 9 V1.

3 TS2G~16GMSA500 TS16G~64GMSA300 Description: 2. Some condition in the host causes the host to issue COMRESET mSATA SSD 1. Host/device is powered and operating normally with some form of active communication. 3. Host releases COMRESET.

Once the condition causing the COMRESET is released, the host releases the COMRESET signal and puts the bus in a quiescent condition. 4. Device issues COMINIT When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT. 5. Host calibrates and issues a COMWAKE. 6. @@@@After ALIGNP Dwords have been sent for 54.6us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed.

If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state. 7. Host locks after detecting the COMWAKE, the host starts transmitting D10.2 characters at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6us (2048 nominal Gen1 Dword times) at any given speed.

@@@@@@8. @@9. @@@@@@@@2. Some condition in the device causes the device to issues a COMINIT 3. Host calibrates and issues a COMWAKE. 4. @@@@@If additional speeds are available, the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword Transcend Information Inc. 11 V1.3 TS2G~16GMSA500 TS16G~64GMSA300 without response from the host, the device enters an error state.

mSATA SSD times.) This step is repeated for as mann. 10. @@@@@@@@@@@@@@@@@@@@Use the SET FEATURES command to specify the mode value. @@Interrupts are not generated on each sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple command. READ SECTOR(S) (20h) This command reads 1 to 256 sectors as specified in the Sector Count register from sectors that is set by Sector number register. A sector count of 0 requests 256 sectors. The transfer beings specified in the Sector Number register. READ VERIFY SECTOR(S) (40h/41h) This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

SET FEATURES (EFh) This command set parameter to Features register and set drive's operation. For transfer mode, parameter is set to Sector Count register. The host to establish or select certain features uses this command. SET MULTIPLE MODE (C6h) This command enables the device to perform READ MULTIPLE and WRITE MULTIPLE operations and establishes the block count for these commands. WRITE DMA (CAh) Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. WRITE MULTIPLE (C5h) This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the Transcend Information Inc. 17 V1.3 TS2G~16GMSA500 TS16G~64GMSA300 WRITE SECTOR(S) (30h) mSATA SSD transfer of a block, which contains the number of sectors defined by Set Multiple command. Write data to a specified number of sectors (1 to 256, as specified with the Sector Count register) from the specified address. Specify "00h" to write 256 sectors. NOP (00h) The device shall respond with command aborted. For devices implementing the Overlapped feature set, subcommand code 00h in the Features register shall abort any outstanding queue. Subcommand codes 01h through FFh in the Features register shall not affect the status of any outstanding queue.

READ BUFFER (E4h) The READ BUFFER command enables the host to read a 512-byte block of data. WRITE BUFFER (E8h) This command enables the host to write the contents of one 512-byte block of data to the device's buffer. Power Management Feature Set CHECK POWER MODE (E5h or 98h) The host can use this command to determine the current power management mode. IDLE (E3h or 97h) This command causes the device to set BSY, enter the "Idle" mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled.

If the sector count is zero, the automatic power mode is disabled. IDLE IMMEDIATE (E1h or 95h) This command causes the device to set BSY, enter the "Idle"(Read) mode, clear BSY and generate an interrupt. SLEEP (E6h or 99h) This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. STANDBY (E2h or 96h) This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately. STANDBY IMMEDIATE (E0h or 94h) This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately. Transcend Information Inc. 18 V1.3 TS2G~16GMSA500 TS16G~64GMSA300 Security Mode Feature Set SECURITY SET PASSWORD (F1h) mSATA SSD This command set user password or master password. The host outputs sector data with PIO data-out protocol to indicate the information defined in the following table. Security set Password data content Word 0 Control word Bit 0 Identifier 0=set user password 1=set master password Bits 1-7 Bit 8 Reserved Security level 0=High 1=Maximum Bits 9-15 1-16 17-255 Reserved Content Password (32 bytes) Reserved SECURITY UNLOCK (F2h) This command disables LOCKED MODE of the device.

This command transfers 512 bytes of data from the host with PIO data-out protocol. The following table defines the content of this information. Security Unlock information Word 0 Control word Bit 0 Identifier 0=compare user password 1=compare master password Bits 1-15 1-16 17-255 Reserved Content Password (32 bytes) Reserved SECURITY DISABLE PASSWORD (F6h) Disables any previously set user password and cancels the lock.

The host transfers 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password. SECURITY ERASE PREPARE (F3h) Transcend Information Inc. 19 V1.

3 TS2G~16GMSA500 TS16G~64GMSA300 This command prevents accidental loss of data on the drive. mSATA SSD This command shall be issued immediately before the Security Erase Unit command to enable erasing and unlocking. SECURITY ERASE UNIT (F4h) The host uses this command to transfer 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive deletes user data, disables the user password, and cancels the lock.

The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password. SECURITY FREEZE LOCK (F5h) Causes the drive to enter Frozen mode. Once this command has been executed, the following commands to update a lock result in the Aborted Command error: · SECURITY SET PASSWORD · SECURITY UNLOCK · SECURITY DISABLE PASSWORD · SECURITY ERASE PREPARE · SECURITY ERASE UNIT The drive exits from Frozen mode upon a power-off or hard reset. If the SECURITY FREEZE LOCK command is issued when the drive is placed in Frozen mode, the drive executes the command, staying in Frozen mode.

SMART Feature Set Transcend IDE SSD supports the SMART command set and define some vendor-specific data to report spare/bad block numbers in each memory management unit. Individual SMART commands are identified by the value placed in the Feature register. Table shows these Feature register values. Value Command D0h SMART READ DATA D2h SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE D4h SMART EXECUTE OFF-LINE IMMEDIATE D8h SMART ENABLE OPERATIONS D9h SMART DISABLE OPERATIONS DAh SMART RETURN STATUS SMART DISABLE OPERATIONS B0h with a Feature register value of D9h.Disables the SMART function. Upon receiving the command, the drive disables all SMART operations. This setting is maintained when the power is turned off and then turns on. Once this command has been received, all SMART commands other than SMART ENABLE OPERATIONS are aborted with the Aborted Command error. Transcend Information Inc. 20 V1.

3 TS2G~16GMSA500 TS16G~64GMSA300 mSATA SSD This command disables all SMART capabilities including any and all timer and event count functions related exclusively to this feature. After command acceptance, this controller will disable all SMART operations. SMART data in no longer be monitored or saved. The state of SMART is preserved across power cycles. SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE B0h with a Feature register value of D2h.Enables or disables the attribute value autosave function. This command specifies whether the current attribute values are automatically saved to the drive when it changes the mode. This setting is maintained when the power is turned on and off. SMART ENABLE OPERATIONS B0h with a Feature register value of D8h.Enables the SMART function.

This setting is maintained when the power is turned off and then turns on. Once the SMART function is enabled, subsequent SMART ENABLE OPERATIONS commands do not affect any parameters SMART EXECUTE OFF-LINE IMMEDIATE B0h with the content of the Features register is equal to D4h. This command causes the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and then save this data to the device's non-volatile memory, or execute a self-diagnostic test routine in either captive or off-line mode. SMART RETURN STATUS B0h with a Feature register value of DAh. @@@@@@This command returns the Device SMART data structure to the host.

@@Users can obtain the data by using the "Read Data" command. Transcend Information Inc. 21 V1.3 TS2G~16GMSA500 TS16G~64GMSA300 Byte 0-1 2 - 361 362 363 364 - 365 366 367 368 - 369 370 371 372 373 374 375 - 385 386 - 395 396 - 397 398 - 399 400 - 406 407 - 415 416 417 418 - 419 420 421 - 423 424 - 425 426 - 428 429 - 431 432 - 445 446 - 510 511 F/V X X V X V X F F X F F F R F F V F X F F V F V V V V F X V mSATA SSD Description Revision code Vender specific Off-line data collection status Self-test execution status byte Total time in second to complete off-line data collection activity Vendor specific Off-line data collection capability SMART capability Error logging capability 7 - 1 Reserved 0 1 = Device error logging supported Vendor specific Short self-test routine recommended polling time (in minutes) Extended self-test routine recommended polling time (in minutes) Conveyance self-test routine recommended polling time (in minutes) Reserved Firmware Version/Date Code Number of initial invalid block (396 = MSB, 397 = LSB) Number of run time bad block (398 = MSB, 399 = LSB) SMI2242' Vendor specific Reserved Program/Write the strong page only Number of spare block Reserved Average erase count Number of child pair Maximum erase count Minimum erase count Reserved Vendor specific Data structure checksum NOTE: F = content (byte) is fixed and does not change. V = content (byte) is variable and may change depending on the state of the device or thr commands executed by the device.

X = content (byte) is vendor specific and may be fixed or variable. R = content (byte) is reserved and shall be zero. N = Nth Management Unit Transcend Information Inc. 22 V1.3 TS2G~16GMSA500 TS16G~64GMSA300 mSATA SSD The above technical information is based on industry standard data and has been tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes to the specifications at any time without prior notice USA Los Angeles: E-mail: sales@transcendusa.com Maryland: E-mail: sales_md@transcendusa.com www.transcendusa.

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