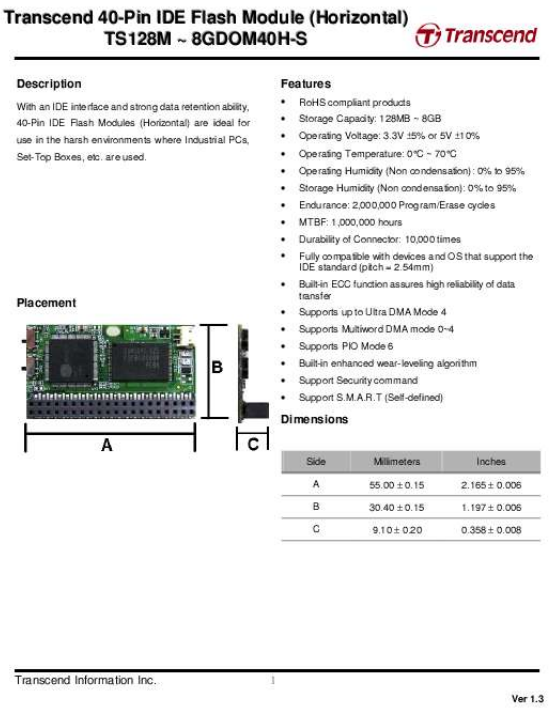

Transcend 40-Pin IDE Flash Module (Horizontal)
TS128M ~ 8GDOM40H-S

Transcend

Description

With an IDE interface and strong data retention ability, 40-Pin IDE Flash Modules (Horizontal) are ideal for use in the harsh environments where Industrial PCs, Set-Top Boxes, etc. are used.

Features

- RoHS compliant products
- Storage Capacity: 128MB ~ 8GB
- Operating Voltage: 3.3V ±5% or 5V ±10%
- Operating Temperature: 0°C ~ 70°C
- Operating Humidity (Non condensation): 0% to 95%
- Storage Humidity (Non condensation): 0% to 95%
- Endurance: 2,000,000 Program/Erase cycles
- MTBF: 1,000,000 hours
- Durability of Connector: 10,000 times
- Fully compatible with devices and OS that support the IDE standard (pitch = 2.54mm)
- Built-in ECC function assures high reliability of data transfer
- Supports up to Ultra DMA Mode 4
- Supports Multiword DMA mode 0~4
- Supports PIO Mode 6
- Built-in enhanced wear-leveling algorithm
- Support Security command
- Support S.M.A.R.T (Self-defined)

Placement

Dimensions

Side	Millimeters	Inches
A	55.00 ± 0.15	2.165 ± 0.006
B	30.40 ± 0.15	1.197 ± 0.006
C	9.10 ± 0.20	0.358 ± 0.008

Transcend Information Inc. 1

Ver 1.3

Manual abstract:

Name No. HD3 HD12 HD2 HD13 HD1 HD14 HD0 HD15 GND VCC Pin Name Pin No. @@@@If Pin 20 of the IDE connector is defined as VCC, then the 40-Pin IDE Flash Module can get necessary power without use of the power cord. 01 -RESET 11 02 GND 12 03 04 05 06 07 08 09 10 HD7 HD8 HD6 HD9 HD5 HD10 HD4 HD11 13 14 15 16 17 18 19 20 21 DMARQ 31 22 GND 32 23 24 25 26 27 28 30 IOWB GND IORB GND IORDY NC GND 33 34 35 36 37 38 40 29 -DMACK 39 Pin Definition Symbol HD0 ~ HD15 HA0 ~ HA2 -RESET IORB IOWB IOIS16B CE1B, CE2B PDIAGB DASPB DMARQ DMACKIREQ NC GND VCC Pin Layout Function Data Bus (Bi-directional) Address Bus (Input) Device Reset (Input) Device I/O Read (Input) Device I/O Write (Input) Transfer Type 8/16 bit (Output) Chip Select (Input) Pass Diagnostic (Bi-directional) Disk Active/Slave Present (Bi-directional) DMA request DMA acknowledge Interrupt Request (Output) No Connection Ground Vcc Power Input Pin2 Pin1 Male Female Bulge Pin39 Pin40 Transcend Information Inc. 2 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S SW1-switch function Master Slave SW2-switch function and Power connector Power connector Write-Protect Disable Transcend Information Inc. 3 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Block Diagram With 1 pcs of Flash Memory: With 2 pcs of Flash Memory: Transcend Information Inc. 4 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S PCB Dimension (unit : mm) TOP Side IDE 40pin Female (Default) TOP Side IDE 40pin Male Transcend Information Inc.

5 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S BOT Side IDE 40pin Female BOT Side IDE 40pin Male Transcend Information Inc. 6 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Absolute Maximum Ratings Symbol VDD-VSS Ta Tst Parameter DC Power Supply Operating Temperature Storage Temperature Min -0.6 0 -40 Max +6 +70 +85 Unit V °C °C DC Characteristics (Ta=0 oC to +70 oC, Vcc = 5.

0V ±10%) Parameter Supply Voltage High level output voltage Low level output voltage High level input voltage Low level input voltage o o Symbol VCC VOH VOL VIH VIL Min 4.5 VCC-0.8 -4.0 2.92 --- Max 5.

5 -0.8 --0.8 1.70 Unit V V V V V V V Remark Non-schmitt trigger Schmitt trigger Schmitt trigger 1 Non-schmitt trigger 1 (Ta=0 C to +70 C, Vcc = 3.3V ±5%) Parameter Supply Voltage High level output voltage Low level output voltage High level input voltage Low level input voltage Symbol VCC VOH VOL VIH VIL Min 3.135 VCC-0.8 -2.4 2.05 --- Max 3.465 -0.

8 --0.6 1.25 Unit V V V V V V V Remark Non-schmitt trigger Schmitt trigger Schmitt trigger 1 Non-schmitt trigger 1 Transcend Information Inc. 7 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Transcend Information Inc. 8 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S True IDE PIO Mode Read/Write Timing Mode Mode Mode Mode Mode Mode Mode 0 1 2 3 4 5 6 1 t0 Cycle time (min) 600 383 240 180 120 100 80 t1 Address Valid to -IORD/-IOWR setup (min) 70 50 30 30 25 15 10 1 t2 -IORD/-IOWR (min) 165 125 100 80 70 65 55 t2 -IORD/-IOWR (min) Register (8 bit) 290 290 290 80 70 65 55 t2i -IORD/-IOWR recovery time (min) ---70 25 25 20 t3 -IOWR data setup (min) 60 45 30 30 20 20 15 t4 -IOWR data hold (min) 30 20 15 10 10 5 5 t5 -IORD data setup (min) 50 35 20 20 20 15 10 t6 -IORD data hold (min) 5 5 5 5 5 5 5 2 t6Z -IORD data tristate (max) 30 30 30 30 30 20 20 4 t7 Address valid to IOCS16 assertion (max) 90 50 40 N/A N/A N/A N/A 4 t8 Address valid to IOCS16 released (max) 60 45 30 N/A N/A N/A N/A t9 -IORD/-IOWR to address valid hold 20 15 10 10 10 10 10 tRD Read Data Valid to IORDY active (min), if 0 0 0 0 0 0 0 IORDY initially low after tA 5 5 tA IORDY Setup time 3 35 35 35 35 35 N/A N/A 5 5 tB IORDY Pulse Width (max) 1250 1250 1250 1250 1250 N/A N/A 5 5 tC IORDY assertion to release (max) 5 5 5 5 5 N/A N/A Notes: All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0 nsec, but minimum -IORD width shall still be met.

Item (1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data.

(2) This parameter specifies the time from the negation edge of -IORD to the time that the data bus is released by the device. (3) The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the device is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time tA after the activation of -IORD or -IOWR, then tRD shall be met and t5 is not applicable.

(4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid. (5) IORDY is not supported in this mode. Transcend Information Inc. 9 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S True IDE PIO Mode Timing Diagram Figure 1: True IDE PIO Mode Timing Diagram Notes: (1) Device address consists of -CS0, -CS1, and A[02::00] (2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit) (3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored. (4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases: (4-1) Device never negates IORDY: No wait is generated.

(4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.

(4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted. Transcend Information Inc. 10 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S True IDE Multiword DMA Mode Read/Write Timing Specification Item Mode 0 (ns) 480 1 Mode 1 (ns) 150 80 60 5 30 15 0 5 50 50 40 40 30 10 25 Mode 2 (ns) 120 70 50 5 20 10 0 5 25 25 35 35 25 10 25 Mode 3 (ns) 100 65 50 5 15 5 0 5 25 25 35 35 10 10 25 Mode 4 (ns) 80 55 45 5 10 5 0 5 20 20 35 35 5 10 25 t0 tD tE tF tG tH tI tJ tKR tKW tLR tLW tM tN tZ Notes: Cycle time (min) 1 -IORD / -IOWR asserted width(min) -IORD data access (max) -IORD data hold (min) -IORD/-IOWR data setup (min) -IOWR data hold (min) DMACK to IORD/-IOWR setup (min) -IORD / -IOWR to -DMACK hold (min) -IORD negated width (min) 1 1 215 150 5 100 20 0 20 50 215 120 40 50 15 20 -IOWR negated width (min) -IORD to DMARQ delay (max) -IOWR to DMARQ delay (max) CS(1:0) valid to IORD / -IOWR CS(1:0) hold -DMACK (1) t0 is the minimum total cycle time and tD is the minimum command active time, while tKR and tKW are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, tD, tKR, and tKW shall be met. The minimum total cycle time requirement is greater than the sum of tD and tKR or tKW .

for input and output cycles respectively. This means a host implementation can lengthen either or both of tD and either of tKR, and tKW as needed to ensure that t0 is equal to or greater than the value reported in the device's identify device data. Transcend Information Inc. 11 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S True IDE Multiword DMA Mode Read/Write Timing Diagram Figure 2: True IDE Multiword DMA Mode Read/Write Timing Diagram Notes: (1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.

(2) This signal may be negated by the host to suspend the DMA transfer in progress. Transcend Information Inc. 12 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Ultra DMA Mode Read/Write Timing Specification Ultra DMA is an optional data transfer protocol used with the READ DMA, and WRITE DMA, commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host.

This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol. TRUE IDE MODE UDMA DMARQ -DMACK STOP1 1,2 -HDMARDY 1,3,4 HSTROBE(W) -DDMARDY(W)1,3 1,2,4 DSTROBE(R) D[15:00] A[02:00]5 -CSEL INTRQ -CS0 -CS1 UDMA Signal DMARQ DMACK STOP HDMARDY(R) HSTROBE(W) DDMARDY(W) DSTROBE(R) DATA ADDRESS CSEL INTRQ Card Select Type Output Input Input Input Output Bidir Input input Output Input Notes: 1) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst. 2) The UDMA interpretation of this signal is valid only during and Ultra DMA data burst during a DMA Read command. 3) The UDMA interpretation of this signal is valid onlDMA Mode 2 Min 240 112 230 15.0 5.0 70.0 6.2 15.0 5.

0 70.0 6.2 0 70.0 0 20 0 20 0 20 160 20 0 20 50 0 20 50 Max Min 160 73 153 10.0 5.0 48.0 6.2 10.0 5.0 48.
0 6.2 0 48.0 0 20 0 20 0 20 125 20 0 20 50 Max Min 120 54 115 7.0 5.0 31.
0 6.2 7.0 5.0 31.0 6.
2 0 31.0 0 20 0 20 0 20 100 20 Max UDMA Mode 3 Min 90 39 86 7.0 5.0 20.0 6.2 7.0 5.0 20.0 6.2 0 20.

0 0 20 0 20 0 20 100 20 0 20 50 Max UDMA Mode 4 Min 60 25 57 5.0 5.0 6.7 6.2 5.0 5.0 6.7 6.2 0 6.7 0 20 0 20 0 20 100 20 0 20 50 Max 230 150 200 150 170 150 130 100 120 100 10 10 10 10 10 70 75 70 70 70 60 55 60 55 60 Measure location (See Note 2) Sender Note 3 Sender Recipient Recipient Sender Sender Device Device Host Host Device Sender Device Note 4 Host Host Note 5 Host Device Host Sender Recipient Device Device Host Sender Notes: All Timings in ns (1) All timing measurement switching points (low to high and high to low) shall be taken at 1.

5 V. (2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and -DMARDY transitions are measured at the sender connector. (3) The parameter tCYC shall be measured at the recipient's connector farthest from the sender. (4) The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively.

Both the incoming signal and the outgoing response shall be measured at the same connector. (5) The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround. (6) See Page 14 the AC Timing requirements in Ultra DMA AC Signal Requirements. Transcend Information Inc. 15 Ver 1.

3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Ultra DMA Data Burst Timing Descriptions Name t2CYCTYP tCYC t2CYC tDS tDH tDVS tDVH tCS tCH tCVS tCVH tZFS tDZFS tFS tLI tMLI tUI tAZ tZAH tZAD tENV tRFS tRP tIORDYZ tZIORDY tACK tSS Comment Notes Typical sustained average two cycle time Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge) Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE) Data setup time at recipient (from data valid until STROBE edge) 2, Data hold time at recipient (from STROBE edge until data may become invalid) 2, Data valid setup time at sender (from data valid until STROBE edge) 3 Data valid hold time at sender (from STROBE edge until data may become invalid) 3 CRC word setup time at device 2 CRC word hold time device 2 CRC word valid setup time at host (from CRC valid until -DMACK negation) 3 CRC word valid hold time at sender (from -DMACK negation until CRC may become 3 invalid) Time from STROBE output released-to-driving until the first transition of critical timing. Time from data output released-to-driving until the first transition of critical timing. First STROBE time (for device to first negate DSTROBE from STOP during a data in burst) Limited interlock time 1 Interlock time with minimum 1 Unlimited interlock time 1 Maximum time allowed for output drivers to release (from asserted or negated) Minimum delay time required for output drivers to assert or negate (from released) Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation) Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY) Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY) Maximum time before releasing IORDY Minimum time before driving IORDY 4, Setup and hold times for -DMACK (before assertion or negation) Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst) Notes: (1) The parameters tUI, tMLI (in Page 19: Ultra DMA Data-In Burst Device Termination Timing and Page 20: Ultra DMA Data-In Burst Host Termination Timing), and tLI indicate sender-to-recipient or recipient-to-sender interlocks,i.

e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding.tUI is an unlimited interlock that has no maximum time value. tMLI is a limited time-out that has a defined minimum. tLI is a limited time-out that has a defined maximum. (2) 80-conductor cabling (see see ATA specification :Annex A)) shall be required in order to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes greater than 2. (3) Timing for tDVS, tDVH, tCVS and tCVH shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value.

Due to reflections on the cable, these timing measurements are not valid in a normally functioning system. (4) For all timing modes the parameter tZIORDY may be greater than tENV due to the fact that the host has a pull-up on IORDY- Transcend Information Inc. 16 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S giving it a known state when released. Ultra DMA Sender and Recipient IC Timing Requirements Name UDMA Mode 0 (ns) UDMA Mode 1 (ns) UDMA Mode 2 (ns) UDMA Mode 3 (ns) UDMA Mode 4 (ns) Min Max Min 9.7 4.8 50.9 9.0 Max Min 6.8 4.
8 33.9 9.0 Max Min 6.8 4.8 22.
6 9.0 Max Min 4.8 4.8 9.5 9.
0 Max tDSIC tDHIC tDVSIC tDVHIC tDSIC tDHIC tDVSIC tDVHIC 14.7 4.8 72.9 9.0 Recipient IC data setup time (from data valid until STROBE edge) (see note 2) Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2) Sender IC data valid setup time (from data valid until STROBE edge) (see note 3) Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3) Notes: (1) All timing measurement switching points(low to high and high to low) shall be taken at 1.5 V. (2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V).

(3) The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values. Ultra DMA AC Signal Requirements Name SRISE SFALL Comment Rising Edge Slew Rate for any signal Falling Edge Slew Rate for any signal Min[V/ns] Max [V/ns] 1.25 1.25 Note 1 1 Note: (1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector. The test load and test points should then be soldered directly to the exposed source side connectors.
The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values. Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope.
The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output Transcend Information Inc. 17 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge. Transcend Information Inc.
18 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Initiating an Ultra DMA Data-In Burst (a) An Ultra DMA Data-In burst is initiated by following the steps lettered below. The timing diagram is shown in below: Ultra DMA Data-In Burst Initiation Timing. The associated timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and are described in Page 13: Ultra DMA Data Burst Timing Descriptions. (b) The following steps shall occur in the order they are listed unless otherwise specifically allowed: (c) The host shall keep -DMACK in the negated state before an Ultra DMA data burst is initiated. (d) The device shall assert DMARQ to initiate an Ultra DMA data burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE. (e) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP. (f) The host shall negate -HDMARDY.

(g) In True IDE mode, the host shall not assert -CS0, -CS1 and A[02:00]. (h) Steps (c), (d), and (e) shall have occurred at least tACK before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA data burst. (i) The host shall release D[15:00] within tAZ after asserting -DMACK. (j) The device may assert DSTROBE tZIORDY after the host has asserted -DMACK. While operating in True IDE mode, once the device has driven DSTROBE, the device shall not release DSTROBE until after the host has negated -DMACK at the end of an Ultra DMA data burst. (k) The host shall negate STOP and assert -HDMARDY within tENV after asserting -DMACK. After negating STOP and asserting -HDMARDY, the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).
(l) The device shall drive D[15:00] no sooner than tZAD after the host has asserted -DMACK, negated STOP, and asserted -HDMARDY. (m) The device shall drive the first word of the data transfer onto D[15:00]. This step may occur when the device first drives D[15:00] in step (j). (n) To transfer the first word of data the device shall negate DSTROBE within tFS after the host has negated STOP and asserted -HDMARDY. The device shall negate DSTROBE no sooner than tDVS after driving the first word of data onto D[15:00].
Transcend Information Inc. 19 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. Notes: The definitions for the IORDY:-DDMARDY:DSTROBE, -IORD: -HDMARDY:HSTROBE, and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are asserted. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions.

Transcend Information Inc. 20 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Sustaining an Ultra DMA Data-In Burst An Ultra DMA Data-In burst is sustained by following the steps lettered below. The timing diagram is shown in below: Sustained Ultra DMA Data-In Burst Timing. @@The following steps shall occur in the order they are listed unless otherwise specifically allowed: a) The device shall drive a data word onto D[15:00]. b) The device shall generate a DSTROBE edge to latch the new word no sooner than tDVS after changing the state of D[15:00]. The device shall generate a DSTROBE edge no more frequently than tCYC for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than 2tcyc for the selected Ultra DMA mode. c) The device shall not change the state of D[15:00] until at least tDVH after generating a DSTROBE edge to latch the data. d) The device shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA data burst is paused, whichever occurs first.

Notes: D[15:00] and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device. Transcend Information Inc. 21 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Host Pausing an Ultra DMA Data-In Burst The host pauses a Data-In burst by following the steps lettered below. A timing diagram is shown in below: Ultra DMA Data-In Burst Host Pause Timing. @@The following steps shall occur in the order they are listed unless otherwise specifically allowed: (a) The host shall not pause an Ultra DMA data burst until at least one data word of an Ultra DMA data burst has been transferred. (b) The host shall pause an Ultra DMA data burst by negating -HDMARDY. (c) The device shall stop generating DSTROBE edges within tRFS of the host negating -HDMARDY. (d) While operating in Ultra DMA modes 2, 1, or 0 the host shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. @@@@(e) The host shall resume an Ultra DMA data burst by asserting -HDMARDY.
ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. @@Notes: (1) The host may assert STOP to request termination of the Ultra DMA data burst no sooner than tRP after -HDMARDY is negated. (2) After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device. (3) The bus polarity of the (-) DMARQ and (-)DMACK signals is dependent on the active interface mode. Transcend Information Inc.
22 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Device Terminating an Ultra DMA Data-In Burst The device terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in below: Ultra DMA Data-In Burst Device Termination Timing. @@The following steps shall occur in the order they are listed unless otherwise specifically allowed: (a) The device shall not pause an Ultra DMA data burst until at least one data word of an Ultra DMA data burst has been transferred. (b) The device shall pause an Ultra DMA data burst by not generating DSTROBE edges.
(c) NOTE - The host shall not immediately assert STOP to initiate Ultra DMA data burst termination when the device stops generating STROBE edges. If the device does not negate DMARQ, in order to initiate Ultra DMA data burst termination, the host shall negate -HDMARDY and wait tRP before asserting STOP. (d) The device shall resume an Ultra DMA data burst by generating a DSTROBE edge. ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. @@Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. Transcend Information Inc. 23 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Host Terminating an Ultra DMA Data-In Burst The host terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in below: Ultra DMA Data-In Burst Host Termination Timing.

@@@@@@@@@@@@@@@@@@@@@@@@@@No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. @@@@@@@@@@@@@@@@@@@@@@@@@@Transcend Information Inc. 24 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S (p) In True IDE mode, the host shall not assert -IORD, -CS0, -CS1, nor A[02:00] until at least tACK after negating DMACK. ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. @@Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. Transcend Information Inc. 25 Ver 1.
3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Initiating an Ultra DMA Data-Out Burst An Ultra DMA Data-out burst is initiated by following the steps lettered below. The timing diagram is shown in below: Ultra DMA Data-Out Burst Initiation Timing. The timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and are described in Page 13:Ultra DMA Data Burst Timing Descriptions. The following steps shall occur in the order they are listed unless otherwise specifically allowed: (a) The host shall keep -DMACK in the negated state before an Ultra DMA data burst is initiated. (b) The device shall assert DMARQ to initiate an Ultra DMA data burst.
(c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP. (d) The host shall assert HSTROBE. (e) In True IDE mode, the host shall not assert -CS0, -CS1, nor A[02:00]. (f) Steps (c), (d), and (e) shall have occurred at least tACK before the host asserts -DMACK.
The host shall keep -DMACK asserted until the end of an Ultra DMA data burst. (g) The device may negate -DDMARDY tZIORDY after the host has asserted -DMACK. While operating in True IDE mode, once the device has negated -DDMARDY, the device shall not release -DDMARDY until after the host has negated DMACK at the end of an Ultra DMA data burst. (h) The host shall negate STOP within tENV after asserting -DMACK. The host shall not assert STOP until after the first negation of HSTROBE. (i) The device shall assert -DDMARDY within tLI after the host has negated STOP. After asserting DMARQ and -DDMARDY the device shall not negate either signal until after the first negation of HSTROBE by the host.

(j) The host shall drive the first word of the data transfer onto D[15:00]. This step may occur any time during Ultra DMA data burst initiation. (k) To transfer the first word of data: the host shall negate HSTROBE no sooner than tUI after the device has asserted -DDMARDY.

The host shall negate HSTROBE no sooner than tDVS after the driving the first word of data onto D[15:00]. Transcend Information Inc. 26 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. @@Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. Transcend Information Inc. 27 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Sustaining an Ultra DMA Data-Out Burst An Ultra DMA Data-Out burst is sustained by following the steps lettered below. The timing diagram is shown in below: Sustained Ultra DMA Data-Out Burst Timing.

The associated timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and are described in Page 13: Ultra DMA Data Burst Timing Descriptions. The following steps shall occur in the order they are listed unless otherwise specifically allowed: (a) The host shall drive a data word onto D[15:00]. (b) The host shall generate an HSTROBE edge to latch the new word no sooner than tDVS after changing the state of D[15:00]. The host shall generate an HSTROBE edge no more frequently than tCYC for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than 2tcyc for the selected Ultra DMA mode.

(c) The host shall not change the state of D[15:00] until at least tDVH after generating an HSTROBE edge to latch the data. (d) The host shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA data burst is paused, whichever occurs first. Note: Data (D[15:00]) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host. Transcend Information Inc. 28 Ver 1.

3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Device Pausing an Ultra DMA Data-Out Burst The device pauses an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram is shown in below: Ultra DMA Data-Out Burst Device Pause Timing. @@The following steps shall occur in the order they are listed unless otherwise specifically allowed: (a) The device shall not pause an Ultra DMA data burst until at least one data word of an Ultra DMA data burst has been transferred. (b) The device shall pause an Ultra DMA data burst by negating -DDMARDY. (c) The host shall stop generating HSTROBE edges within tRFS of the device negating -DDMARDY. (d) While operating in Ultra DMA modes 2, 1, or 0 the device shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words. @@(e) The device shall resume an Ultra DMA data burst by asserting -DDMARDY. ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. @@Notes: (1) The device may negate DMARQ to request termination of the Ultra DMA data burst no sooner than tRP after -DDMARDY is negated.

(2) After negating -DDMARDY, the device may receive zero, one, two, or three more data words from the host. Transcend Information Inc. 29 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Device Terminating an Ultra DMA Data-Out Burst The device terminates an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram for the operation is shown in below: Ultra DMA Data-Out Burst Device Termination Timing. @@The following steps shall occur in the order they are listed unless otherwise specifically allowed: (a) The device shall not initiate Ultra DMA data burst termination until at least one data word of an Ultra DMA data burst has been transferred. (b) The device shall initiate Ultra DMA data burst termination by negating -DDMARDY. (c) The host shall stop generating an HSTROBE edges within tRFS of the device negating -DDMARDY. (d) While operating in Ultra DMA modes 2, 1, or 0 the device shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words.

@@(e) The device shall negate DMARQ no sooner than tRP after negating -DDMARDY. @@(f) The host shall assert STOP within tLI after the device has negated DMARQ. @@(g) If HSTROBE is negated, the host shall assert HSTROBE within tLI after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE.

HSTROBE shall remain asserted until the Ultra DMA data burst is terminated. (h) The host shall place the result of its CRC calculation on D[15:00] (see ATA specification Ultra DMA CRC Calculation). (i) The host shall negate -DMACK no sooner than tMLI after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than tDVS after placing the result of its CRC calculation on D[15:00]. (j) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK. (k) The device shall compare the CRC data received from the host with the results of its own CRC calculation.

If a miscompare error occurs during one or more Ultra DMA data bursts for any one command, the device shall report the first error that occurred (see ATA specification Ultra DMA CRC Calculation). (l) While operating in True IDE mode, the device shall release DSTROBE within tIORDYZ after the host negates -DMACK. (m) The host shall not negate STOP nor assert HDMARDY until at least tACK after negating -DMACK. (n) In True IDE mode, the host shall not assert -IOWR, -CS0, -CS1, nor A[02:00] until at least tACK after negating DMACK. Transcend Information Inc. 30 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. @@Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A00-A02, -CS0 & -CS1 are True IDE mode signal definitions.

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31 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Host Terminating an Ultra DMA Data-Out Burst Termination of an Ultra DMA Data-Out burst by the host is shown in below: Ultra DMA Data-Out Burst Host Termination Timing while timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and timing parameters are described in Page 13: Ultra DMA Data Burst Timing Descriptions. The following steps shall occur in the order they are listed unless otherwise specifically allowed: (a) The host shall initiate termination of an Ultra DMA data burst by not generating HSTROBE edges. (b) The host shall assert STOP no sooner than tSS after it last generated an HSTROBE edge. (c) The device shall negate DMARQ within tLI after the host asserts STOP. @@(d) The device shall negate -DDMARDY within tLI after the host has negated STOP. The device shall not assert -DDMARDY again until after the Ultra DMA data burst termination is complete. (e) If HSTROBE is negated, the host shall assert HSTROBE within tLI after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE.
HSTROBE shall remain asserted until the Ultra DMA data burst is terminated. (f) The host shall place the result of its CRC calculation on D[15:00] (see ATA specification Ultra DMA CRC Calculation). (g) The host shall negate -DMACK no sooner than tMLI after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than tDVS after placing the result of its CRC calculation on D[15:00]. (h) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK. (i) The device shall compare the CRC data received from the host with the results of its own CRC calculation.
If a miscompare error occurs during one or more Ultra DMA data bursts for any one command, at the end of the command, the device shall report the first error that occurred (see ATA specification Ultra DMA CRC Calculation). @@@@@@@@Notes: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. Transcend Information Inc. 33 Ver 1.
3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S IDENTIFY DEVICE information The Identify Device command enables the host to receive parameter information from the device. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table as below. All reserved bits or words are zero. Hosts should not depend on Obsolete words in Identify Device containing 0. Table below specifies each field in the data returned by the Identify Device Command. In Table as below, X indicates a numeric nibble value specific to the card and aaaa indicates an ASCII string specific to the particular drive. Word Address Default Value Total Bytes Data Field Type Information 0 1 2 3 4 5 6 7-8 9 10-19 20 21 22 23-26 27-46 47 48 49 50 044Ah XXXXh 0000h 00XXh 0000h 0000h XXXXh XXXXh XXXXh aaaa 0000h 0000h 0004h aaaa aaaa XXXXh 0000h XX00h 0000h 2 2 2 2 2 2 2 4 2 20 2 2 2 8 40 2 2 2 2 General configuration Bit Significant with ATA-4 definitions. Default number of cylinders Reserved Default number of heads Obsolete Obsolete Default number of sectors per track Number of sectors per card (Word 7 = MSW, Word 8 = LSW) Obsolete Serial number in ASCII (Right Justified) Obsolete Obsolete Number of ECC bytes passed on Read/Write Long Commands Firmware revision in ASCII. Big Endian Byte Order in Word Model number in ASCII (Left Justified) Big Endian Byte Order in Word Maximum number of sectors on Read/Write Multiple command Reserved Capabilities Reserved Transcend Information Inc.

34 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Word Address Default Value Total Bytes Data Field Type Information 51 52 53 54 55 56 57-58 59 60-61 62 63 64 65 66 67 68 69-79 80-81 82-84 85-87 88 89 90 91 92-127 128 129-159 160 161 162 163 164 165-167 168-255 0200h 0000h 000Xh XXXXh XXXXh XXXXh XXXXh 01XXh XXXXh 0000h 0X0Xh 0003h XXXXh XXXXh XXXXh XXXXh 0000h 0000h XXXXh XXXXh 001Fh XXXXh XXXXh XXXXh 0000h XXXXh 0000h XXXXh 0000h 0000h XXXXh XXXXh 0000h 0000h 2 2 2 2 2 2 2 4 2 4 2 2 2 2 2 2 2 2 20 4 6 6 2 2 2 2 72 2 64 2 2 2 2 2 6 158 PIO data transfer cycle timing mode Obsolete Field Validity Current numbers of cylinders Current numbers of heads Current sectors per track Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW) Multiple sector setting Total number of sectors addressable in LBA Mode Reserved Multiword DMA transfer. In PC Card modes this value shall be 0h Advanced PIO modes supported Minimum Multiword DMA transfer cycle time per word. In PC Card modes this value shall be 0h Recommended Multiword DMA transfer cycle time. In PC Card modes this value shall be 0h Minimum PIO transfer cycle time without flow control Minimum PIO transfer cycle time with IORDY flow control Reserved Reserved CF cards do not return an ATA version Features/command sets supported Features/command sets enabled Ultra DMA Mode Supported and Selected (UDMA mode 0 ~ 4) Time required for Security erase unit completion Time required for Enhanced security erase unit completion Current Advanced power management value Reserved Security status Vendor unique bytes Power requirement description Reserved for assignment by the CFA Key management schemes supported CF Advanced True IDE Timing Mode Capability and Setting CF Advanced PC Card I/O and Memory Timing Mode Capability Reserved for assignment by the CFA Reserved 35 Ver 1.3 Transcend Information Inc. Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Command Set Command 1 2 3 4 5 6 7 8 9 10 Check Power Mode Execute Drive Diagnostic Erase Sector Flush Cache Format Track Identify Device Idle Idle Immediate Initialize Drive Parameters Key Management Structure Read Code E5 or 98h 90h C0h E7h 50h ECh E3h or 97h E1h or 95h 91h B9 (Feature 0-127) FR Y SC Y Y Y Y Y SN Y Y CY Y Y Y DH Y Y Y Y Y Y Y Y Y Y LBA Y Y Status Support Support Support Not Support Support Support Support Support Support NOT Support #1 #3 Note 11 Key Management Read Keying Material Key Management Change Key Management Value NOP Read Buffer Read DMA Read Long Sector Read Multiple Read Sector(s) Read Verify Sector(s) Recalibrate Request Sense Security Disable Password Security Erase Prepare Security Erase Unit Security Freeze Lock Security Set Password B9 (Feature 80) Y Y Y Y Y NOT Support #1 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 B9 (Feature 81) 00h E4h C8h 22h or 23h C4h 20h or 21h 40h or 41h 1Xh 03h F6h F3h F4h F5h F1h Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y NOT Support NOT Support Support Support NOT Support Support Support Support Support #1 #2 Y Y Y Y Y Y Support Support Support Support Support Support Transcend Information Inc.

36 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 Security Unlock Seek Set Feature Set Multiple Mode Set Sleep Mode Standby Standby Immediate Translate Sector Wear Level Write Buffer Write DMA Write Long Sector Write Multiple Write Multiple w/o Erase Write Sector(s) Write Sector(s) w/o Erase Write Verify F2h 7Xh EFh C6h E6h or 99h E2 or 96h E0 or 94h 87h F5h E8h CAh 32h or 33h C5h CDh 30h or 31h 38h 3Ch Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Y Support Support Support Support Support Support Support Support Support Support Not Support Support Support Support Support #2 #1: This command is optional, depending on the key Management scheme in use. #2: Use of this command is not recommended.

#3: The controller doesn't have cache. Definitions FR = Features Register SC =Sector Count register (00H to FFH, 00H means 256 sectors) SN = Sector Number register CY = Cylinder Low/High register DH = Head No. (0 to 15) of Drive/Head register LBA = Logic Block Address Mode Support = Not used for the command Y = Used for the command Transcend Information Inc. 37 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S SMART Command Set SMART Command Set SMART Feature Register Values D0h D1h D2h D3h Read Data Read Attribute Threshold Enable/Disable Autosave Save Attribute Values D4h D8h D9h DAh Execute OFF-LINE Immediate Enable SMART Operations Disable SMART Operations Return Status 1.

If reserved size is below the Threshold, the status can be read from Cylinder register by Return Status command (DAh). SMART Data Structure BYTE 0-1 2-361 362 363 364-365 366 367 368-369 370 F/V X X V X V X F F F Revision code Vendor specific Off line data collection status Self-test execution status byte Total time in seconds to complete off-line data collection activity Vendor specific Off-line data collection capability SMART capability Error logging capability 7-1 Reserved 0 1=Device error logging supported 371 372 373 374 375-385 386-395 396 397+(n*6) 398+(n*6) 400+(n*6) X F F F R F V V V V Vendor specific Short self-test routine recommended polling time (in minutes) Extended self-test routine recommended polling time (in minutes) Conveyance self-test routine recommended polling time (in minutes) Reserved Date Code Number of MU in device (0~n) MU number MU data block MU spare block 38 Ver 1.3 Decription Transcend Information Inc. Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S 401+(n*6) 402+(n*6) 511 V V V Init. Bad block Last Defect Bad block (Newest state) Data structure checksum F=the content of the byte is fixed and does not change.

V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device. X=the content of the byte is vendor specific and may be fixed or variable. R=the content of the byte is reserved and shall be zero. * 4 Byte value : [MSB] [2] [1] [LSB] Capacity Specifications: Transcend P/N TS128MDOM40H-S TS256MDOM40H-S TS512MDOM40H-S TS1GDOM40H-S TS2GDOM40H-S TS4GDOM40H-S TS8GDOM40H-S Capacity 128MB 256MB 512MB 1GB 2GB 4GB 8GB Cylinder (C) 248 496 993 1942 3884 7769 15538 Head (H) 16 16 16 16 16 16 16 Sector (S) 63 63 63 63 63 63 63 Transcend Information Inc. 39 Ver 1.3 Transcend 40-Piin IIDE Fllash Modulle (Horiizontall) Transcend 40-P n DE F ash Modu e (Hor zonta) TS128M ~ 8GDOM40H-S TS128M ~ 8GDOM40H-S Ordering Information TS XXXX DOM 40 X-S Transcend Product Capacity: 128M-512M = 128 MB up to 512 MB 1G-8G = 1 GB up to 8 GB IDE Flash Module (Disk On Module) Type: V = Vertical H = Horizontal Pin Count: 40 = 40 pin 44 = 44 pin The above technical information is based on industry standard data and has been tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes to the specifications at any time without prior notice. USA Los Angeles: E-mail: sales@transcendusa.com Maryland: E-mail: sales_md@transcendusa.

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