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You can read the recommendations in the user guide, the technical guide or the installation guide for MAXTOR DIAMONDMAX PLUS 40. You'll find the answers to all your questions on the MAXTOR DIAMONDMAX PLUS 40 in the user manual (information, specifications, safety advice, size, accessories, etc.). Detailed instructions for use are in the User's Guide.

User manual MAXTOR DIAMONDMAX PLUS 40
User guide MAXTOR DIAMONDMAX PLUS 40
Operating instructions MAXTOR DIAMONDMAX PLUS 40
Instructions for use MAXTOR DIAMONDMAX PLUS 40
Instruction manual MAXTOR DIAMONDMAX PLUS 40

DiamondMax™ Plus 40
54058LR, 53073LUS, 53049RH,
51538L3, 510E4L2

Part # 1428/A

Maxtor®

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Manual abstract:

@@@ Contents and specifications subject to change without notice. @@ This manual provides technical information for OEM engineers and systems integrators regarding the installation and use of DiamondMax hard drives. Drive repair should be performed only at an authorized repair center. For repair information, contact the Maxtor Customer Service Center at 800-2MAXTOR or 408-922-2085. Before unpacking the hard drive, please review Sections 1 through 4. C A U T I O N Maxtor DiamondMax Plus 40 hard drives are precision products. Failure to follow these precautions and guidelines outlined here may lead to product failure, damage and invalidation of all warranties. 1 2 3 4 5 6 BEFORE unpacking or handling a drive, take all proper electro-static discharge (ESD) precautions, including personnel and equipment grounding. Stand-alone drives are sensitive to ESD damage. BEFORE removing drives from their packing material, allow them to reach room temperature.

During handling, NEVER drop, jar, or bump a drive. Once a drive is removed from the Maxtor shipping container, IMMEDIATELY secure the drive through its mounting holes within a chassis. Otherwise, store the drive on a padded, grounded, antistatic surface. NEVER switch DC power onto the drive by plugging an electrically live DC source cable into the drive's connector. NEVER connect a live bus to the drive's interface connector.

ELECTRICAL GROUNDING - For proper operation, the drive must be securely fastened to a device bay that provides a suitable electrical ground to the drive baseplate. Please do not remove or cover up Maxtor factory-installed drive labels. They contain information required should the drive ever need repair.

DIAMONDMAX PLUS 40 PRODUCT MANUAL Contents Section 1 -- Introduction Maxtor Corporation Products Support Manual Organization Abbreviations Conventions Key Words Numbering Signal Conventions 1-1 1-1 1-1 1-1 1-1 1-2 1-2 1-2 1-2 Section 2 -- Product Description The DiamondMax® Plus 40 Product Features Functional/Interface Zone Density Recording Read/Write Multiple Mode UltraDMA - Mode 4 Multi-word DMA (EISA Type B) - Mode 2 Sector Address Translation Logical Block Addressing Defect Management Zone On-the-Fly Hardware Error Correction Code (ECC) Software ECC Correction Automatic Head Park and Lock Operation Cache Management Buffer Segmentation Read-Ahead Mode Automatic Write Reallocation (AWR) Write Cache Stacking Major HDA Components Drive Mechanism Rotary Actuator Read/Write Electronics Read/Write Heads and Media Air Filtration System Microprocessor Subsystem Configuration Dual Drive Support Cable Select Option Jumper Location/Configuration Cylinder Limitation 2-2 2-2 2-2 2-2 2-2 2-2 2-2 2-3 2-3 2-3 2-3 2-3 2-4 2-4 2-4 2-4 2-5 2-5 2-5 2-5 2-5 2-5 2-6 2-6 2-6 2-6 2-6 i DIAMONDMAX PLUS 40 PRODUCT MANUAL Section 3 -- Product Specifications Models and Capacities Drive Configuration Performance Specifications Physical Dimensions Power Requirements Power Mode Definitions Spin-up Seek Read/Write Idle Standby Sleep EPA Energy Star Compliance Environmental Limits Shock and Vibration Reliability Specifications Annual Return Rate Quality Acceptance Rate Start/Stop Cycles Data Reliability Component Design Life EMC/EMI EMC Compliance Canadian Emissions Statement Safety Regulatory Compliance 3-1 3-1 3-1 3-2 3-3 3-3 3-3 3-3 3-3 3-3 3-3 3-3 3-4 3-4 3-4 3-4 3-4 3-4 3-4 3-5 3-5 3-5 3-5 Section 4 -- Handling and Installation Hard Drive Handling Precautions Electro-Static Discharge (ESD) Unpacking and Inspection Repacking Physical Installation Before You Begin Please Read Back up. Protect Your Existing Data Tools for Installation System Requirements Operating System Requirements Hook up Boot the System with MaxBlast Plus Diskette Configure the Drive Jumpers Installing 5.

25-inch Mounting Brackets Install Hard Drive in Device Bay Attach Interface and Power Cables Start up Set up 4-1 4-1 4-2 4-3 4-3 4-4 4-4 4-4 4-4 4-4 4-4 4-4 4-4 4-5 4-5 4-5 4-5 ii DIAMONDMAX PLUS 40 PRODUCT MANUAL Section 5 -- AT Interface Description Interface Connector Pin Description Summary Pin Description Table PIO Timing DMA Timing Ultra DMA Timing Parameters 5-1 5-1 5-2 5-3 5-4 5-5 Section 6 -- Host Software Interface Task File Registers Data Register Error Register Features Register Sector Count Register Sector Number Register Cylinder Number Registers Device/Head Register Status Register Command Register Read Commands Write Commands Mode Set/Check Commands Power Mode Commands Initialization Commands Seek, Format, and Diagnostic Commands S.M.A.R.T. Commands Summary Control Diagnostic Registers Alternate Status Register Device Control Register Digital Input Register Reset and Interrupt Handling 6-1 6-1 6-1 6-1 6-2 6-2 6-2 6-2 6-2 6-2 6-3 6-3 6-3 6-3 6-3 6-3 6-3 6-3 6-4 6-5 6-5 6-5 6-6 Section 7 -- Interface Commands Command Summary Read Commands Read Sector(s) Read Verify Sector(s) Read Sector Buffer Read DMA Read Multiple Set Multiple Write Commands Write Sector(s) 7-1 7-2 7-2 7-2 7-2 7-3 7-3 7-3 7-4 7-4 iii DIAMONDMAX PLUS 40 PRODUCT MANUAL Write Verify Sector(s) Write Sector Buffer Write DMA Write Multiple Ultra DMA Set Feature Commands Set Features Mode Power Mode Commands Standby Immediate Idle Immediate Standby Idle Check Power Mode Set Sleep Mode Default Power-on Condition Initialization Commands Identify Drive Initialize Drive Parameters Seek, Format, and Diagnostic Commands S.M.A.R.T.

Command Set 7-4 7-4 7-5 7-5 7-5 7-5 7-5 7-7 7-7 7-7 7-7 7-7 7-7 7-7 7-9 7-9 7-9 - 12 7-13 7-14 8-1 8-1 8-1 Section 8 -- Service and Support Service Policy No Quibble Service Support Glossary iv DIAMONDMAX PLUS 40 PRODUCT MANUAL Figures Figure 2-1 3-1 4-1 4-2 4-3 4-4 4-5 4-6 4-7 5-1 5-2 5-3 5-4 5-5 5-6 5-7 5-8 5-9 5-10 5-11 5-12 5-13 Title PCBA Jumper Location and Configuration Outline and Mounting Dimensions Multi-pack Shipping Container Single-pack Shipping Container (Option A) Single-pack Shipping Container (Option B) Master, Slave and Cable Select Settings 5.25-inch Mounting Brackets and Rails IDE Interface and Power Cabling Detail Master, Slave and Cable Select Settings Data Connector PIO Data Transfer to/from Device Multi-word DMA Data Transfer Initiating an Ultra DMA Data In Burst Sustained Ultra DMA Data In Burst Host Pausing an Ultra DMA Data In Burst Device Terminating an Ultra DMA Data In Burst Host Terminating an Ultra DMA Data In Burst Initiating an Ultra DMA Data Out Burst Sustained Ultra DMA Data Out Burst Device Pausing an Ultra DMA Data Out Burst Host Terminating an Ultra DMA Data Out Burst Device Terminating an Ultra DMA Data Out Burst Page 2-6 3-2 4-2 4-3 4-3 4-5 4-6 4-7 4-10 5-1 5-3 5-4 5-5 5-6 5-6 5-7 5-7 5-8 5-8 5-9 5-9 5-10 v DIAMONDMAX PLUS 40 INTRODUCTION SECTION 1 Introduction Maxtor Corporation Maxtor Corporation has been providing high-quality computer storage products since 1982. Along the way, we've seen many changes in data storage needs.



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Not long ago, only a handful of specific users needed more than a couple hundred megabytes of storage. Today, downloading from the Internet and CD-ROMs, multimedia, networking and advanced office applications are driving storage needs even higher. Even home PC applications need capacities measured in gigabytes, not megabytes. Products Maxtor's products meet demanding storage capacity requirements with room to spare. They feature proven compatibility and reliability. While DiamondMax® Plus 40 is the latest addition to our legacy of high performance 7,200 RPM desktop and workstation hard drives, our DiamondMax® VL 20 series hard drives deliver industry-leading capacity, reliability and value for entry-level systems and consumer electronics applications. Support No matter which capacity, all Maxtor hard drives are supported by our commitment to total customer satisfaction and our No Quibble Service® guarantee.

One call or a visit to our home page on the Internet (<http://www.maxtor.com>) puts you in touch with either technical support or customer service. We'll provide you the information you need quickly, accurately and in the form you prefer - a fax, a downloaded file or a conversation with a representative. Manual Organization This hard disk drive reference manual is organized in the following method: Section 1 Section 2 Section 3 Section 4 Section 5 Section 6 Section 7 Section 8 Appendix Introduction Description Specifications Installation AT Interface Host Software Interface Interface Commands Service and Support

Glossary Abbreviations A B B R V D E S C R I P T I O N ATA AT attachment bpi bits per inch C H S cylinder - head - sector dBA decibels dBA weighted D M A direct memory access ECC error correction code fci flux changes per inch G a c c e l e r a t i o n GB gigabyte H z h e r t z KB kilobyte LBA logical block address(ing) LSB least significant bit m A m illia m p e r e s A B B R V D E S C R I P T I O N MB megabyte M b i t s / s e c m e g a b i t s p e r s e c o n d MB/sec megabytes per second M H z m e g a h e r t z m s m illis e c o n d M S B m o s t s i g n i f i c a n t b i t mV millivolts n s n a n o s e c o n d s P I O p r o g r a m m e d i n p u t / o u t p u t RPM revolutions per minute tpi tracks per inch U D M A u l t r a d i r e c t m e m o r y a c c e s s μ s e c m i c r o s e c o n d V volts W watts 11 DIAMONDMAX PLUS 40 INTRODUCTION Conventions If there is a conflict between text and tables, the table shall be accepted as being correct.

Key Words The names of abbreviations, commands, fields and acronyms used as signal names are in all uppercase type (e.g., IDENTIFY DRIVE). Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. Names of drive registers begin with a capital letter (e.g., Cylinder High register). Numbering Numbers that are not followed by a lowercase "b" or "h" are decimal values. Numbers that are followed by a lowercase "b" (e.g., 01b) are binary values. Numbers that are followed by a lowercase "h" (e.g., 3Ah) are hexadecimal values. Signal Conventions Signal names are shown in all uppercase type.

All signals are either high active or low active signals. A dash character (-) at the end of a signal name indicates that the signal is low active. A low active signal is true when it is below ViL and is false when it is above ViH. A signal without a dash at the end indicates that the signal is high active. A high active signal is true when it is above ViH and is false when it is below ViL. When a signal is asserted, it means the signal is driven by an active circuit to its true state. When a signal is negated, it means the signal is driven by an active circuit to its false state. When a signal is released, it means the signal is not actively driven to any state. Some signals have bias circuitry that pull the signal to either a true or false state when no signal driver is actively asserting or negating the signal. These instances are noted under the description of the signal.

12 PRODUCT DESCRIPTION SECTION 2 Product Description Maxtor DiamondMax® Plus 40 AT disk drives are 1-inch high, 3.5-inch diameter random access storage devices which incorporate an on-board ATA-5/Ultra DMA 66 controller. High capacity is achieved by a balanced combination of high areal recording density and the latest data encoding and servo techniques. Maxtor's latest advancements in electronic packaging and integration methods have lowered the drive's power consumption and increased its reliability. Advanced giant magneto-resistive read/write heads and a state-of-the-art head/disk assembly - using an integrated motor/spindle design - allow up to four disks in a 3.5-inch package. Exceptionally high data transfer rates, 7,200 RPM spin speed and < 9.0 ms access times make these performance series disk drives especially well-suited to high-end dHSPT = Host Sectors per Track (1) (2) 22 PRODUCT DESCRIPTION The LBA is checked for violating the drive capacity. If it does not, the LBA is converted to physical drive cylinder, head and sector values. The physical address is then used to access or store the data on the disk and for other drive related operations.

Defect Management Zone (DMZ) Each drive model has a fixed number of spare sectors per drive, all of which are located at the end of the drive. Upon detection of a bad sector that has been reassigned, the next sequential sector is used. For example, if sector 3 is flagged, data that would have been stored there is "pushed down" and recorded in sector 4. Sector 4 then effectively becomes sector 3, as sequential sectors are "pushed down" across the entire drive. The first spare sector makes up for the loss of sector 3, and so maintains the sequential order of data. This push down method assures maximum performance.

On-the-Fly Hardware Error Correction Code (ECC) 5 symbols, single burst, guaranteed Software ECC Correction 22 symbols, single burst, guaranteed Automatic Park and Lock Operation Immediately following power down, dynamic braking of the spinning disks delays momentarily allowing the read/write heads to move to an inner mechanical stop. A small fixed magnet holds the rotary actuator in place as the disk spins down. The rotary actuator is released only when power is again applied. Cache Management Buffer Segmentation The data buffer is organized into two segments: the data buffer and the micro controller scratch pad.

The data buffer is dynamically allocated for read and write data depending on the commands received. A variable number of read and write buffers may exist at the same time. Read-Ahead Mode Normally, this mode is active. Following a read request, disk read-ahead begins on the first sector and continues sequentially until the allocated buffer is full.



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If a read request is received during the read-ahead operation, the buffer is examined to determine if the request is in the cache. If a cache hit occurs, readahead mode continues without interruption and the host transfer begins immediately. Automatic Write Reallocation (AWR) This feature is part of the write cache and reduces the risk of data loss during deferred write operations. If a disk error occurs during the disk write process, the disk task stops and the suspect sector is reallocated to a pool of alternate sectors located at the end of the drive. Following reallocation, the disk write task continues until it is complete. Write Cache Stacking Normally, this mode is active.

Write cache mode accepts the host write data into the buffer until the buffer is full or the host transfer is complete. A command complete interrupt is generated at the end of the transfer. A disk write task begins to store the host data to disk. @@The drive may reorder write commands to optimize drive throughput. 23

PRODUCT DESCRIPTION Major HDA Components Drive Mechanism A brush-less DC direct drive motor rotates the spindle at 7,200 RPM ($\pm 0.1\%$). The dynamically balanced motor/spindle assembly ensures minimal mechanical run-out to the disks. A dynamic brake provides a fast stop to the spindle motor upon power removal. The speed tolerance includes motor performance and motor circuit tolerances. Rotary Actuator All DiamondMax Plus 40 drives employ a rotary voice coil actuator which consists of a moving coil, an actuator arm assembly and stationary magnets.

The actuator moves on a low-mass, low-friction center shaft. The low friction contributes to fast access times and low power consumption. Read/Write Electronics An integrated circuit mounted within the sealed head disk assembly (near the read/write heads) provides up to eight head selection (depending on the model), read pre-amplification and write drive circuitry. Read/Write Heads and Media Low mass, low force giant magneto-resistive read/write heads record data on 3.5-inch diameter disks. Maxtor uses a sputtered thin film medium on all disks for DiamondMax Plus 40 drives. Air Filtration System All DiamondMax Plus 40 drives are assembled in a Class 100 controlled environment. Over the life of the drive, a 0.1 micron filter and breather filter located within the sealed head disk assembly (HDA) maintain a clean environment to the heads and disks. DiamondMax 40 drives are designed to operate in a typical office environment with minimum environmental control.

Microprocessor The microprocessor controls the following functions for the drive electronics: Command execution Cache management Data correction and error recovery Diagnostic execution Data sequencing Head positioning (including error recovery) Host interface Index detection Spin speed control Seeks Servo S.M.A.R.T. 24 **PRODUCT DESCRIPTION Subsystem Configuration Dual Drive Support** Two drives may be accessed via a common interface cable, using the same range of I/O addresses. The drives are jumpered as device 0 or 1 (Master/Slave), and are selected by the drive select bit in the Device/Head register of the task file. All Task File registers are written in parallel to both drives. The interface processor on each drive decides whether a command written to it should be executed; this depends on the type of command and which drive is selected. Only the drive selected executes the command and activates the data bus in response to host I/O reads; the drive not selected remains inactive.

A master/slave relationship exists between the two drives: device 0 is the master and device 1 the slave. When J50 is closed (factory default, figure 2-1), the drive assumes the role of master; when open, the drive acts as a slave. In single drive configurations, J50 must be closed. Cable Select Option CSEL (cable select) is an optional feature per ANSI ATA specification. Drives configured in a multiple drive system are identified by CSEL's value: If CSEL is grounded, then the drive address is 0.

If CSEL is open, then the drive address is 1. Jumper Location / Configuration Darkened jumper pins indicate factory-installed (default) shunts. +12 VDC +12 V return +5 V return EIDE Interface Connector J1 pin 1 +5 VDC JUMPER CONFIGURATION Master/Slave Only drive in single drive system* Master drive in dual drive system* Slave drive in dual drive system C a b l e S e l e c t D i s a b l e d * E n a b l e d Power Connector J2 J50 C C O J48 J46 J44 J42 O C O C J50 - Master/Slave J48 - Cable Select J46 - Cylinder Limitation J44 - Factory Reserved J42 - Factory Reserved Cylinder Limitation D i s a b l e d * E n a b l e d F a c t o r y R e s e r v e d O F a c t o r y R e s e r v e d O K e y * = D e f a u l t C = C l o s e d (jumper installed) O = O p e n (no jumper installed) Figure 2-1 PCBA Jumper Location and Configuration Cylinder Limitation Jumper Description On some older BIOS', primarily those that auto-configure the disk drive, a hang may occur. The Cylinder Limitation jumper reduces the capacity in the Identify Drive allowing large capacity drives to work with older BIOS'. The capacity reported when J46 is closed will be as follows: drives less than or equal to 32GB will report 2.

1GB. Drives greater than 32GB will report 32GB. 25 **PRODUCT SPECIFICATIONS SECTION 3 Product Specifications Models and Capacities MODEL Formatted Capacity (MB LBA Mode)** 54098U8 40,980 53073U6 30,735 52049U4 20,490 51536U3 15,367 51024U2 10,245 Maxtor defines one megabyte as 106 or one million bytes and one gigabyte as 109 or one billion bytes. Drive Configuration MODEL Integrated Controller / Interface Encoding Method Interleave Servo System Buffer Size / Type Data Zones per Surface Data Surfaces / Heads Number of Disks Areal Density Track Density Recording Density Flux Density Bytes per Sector / Block Sectors per Track Sectors per Drive 80,041,248 60,030,432 8 4 6 3 5 4 0 9 8 U8 5 3 0 7 3 U6 5 2 0 4 9 U4 5 1 5 3 6 U3 5 1 0 2 4 U2 ATA-5 / Ultra DMA E2 PR4 RLL 16/17 1:1 Embedded 2 MB SDRAM 16 4 2 7 245 Gb / in2 max . 21,500 tpi 270 - 337 kbp 286 - 358 kfc 512 325 - 560 40,020,624 30,015,216 20,010,816 3 2 2 1 Performance Specifications MODEL Seek Times (typical read) Track-to-Track Average Full Stroke Average Latency Rotational Speed ($\pm 0.1\%$) Controller Overhead Data Transfer Rate To/From Interface (UltraDMA - M4) To/From Interface (PIO 4/Multi-word DMA M4) To/From Media Start Time (0 to Drive Ready) up to 66.0 MB/sec up to 16.7 MB/sec up to 43.2 MB/sec < 10 sec typical 1.0 ms < 9.

0 ms < 20.0 ms 4.17 ms 7 200 RPM , < 0.3 ms 5 4 0 9 8 U8 5 3 0 7 3 U6 5 2 0 4 9 U4 5 1 5 3 6 U3 5 1 0 2 4 U2 31 **PRODUCT SPECIFICATIONS Physical Dimensions (maximum) PARAMETER Height Length Width Weight STANDARD** 1.028 inches 5.787 inches 4.00 inches 1.3 pounds METRIC 26.1 millimeters 147 millimeters 101.6 millimeters 0.59 kilograms 1.028 max [26.1 mm max 6 x 6-32 UNC -28 THREAD 1.



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638 ± .010 [41.
6 ± 0.25 mm] 4.00 ± .01 [101.6 ± 0.
5 mm] 1.122 ± .020 [28.5 ± 0.5 mm] .25 ± .01 [6.35 ± 0.25 mm 5.787 max [147 mm max] 4 x 6-32 UNC -28 THREAD 1.

75 ± .01 [44.95 ± 0.25 mm] 1.625 ± .02 [41.28 ± 0.5 mm] 3.75 ± .01 [95.
25 ± 0.25 mm] .125 ± .010 [3.18 ± .

025 mm] Figure 3 - 1 Outline and Mounting Dimensions 32 4.00 ± .01 [101.6 ± 0.25 mm] PRODUCT SPECIFICATIONS Power Requirements MODE Spin-up (peak) Seek (avg) Read/Write (avg) Idle (avg) Standby (avg) Sleep (avg) 12V ± 10% 250 0 mA 80 0 mA 350 mA 350 mA 15 mA 15 mA 5V ± 5% 620 mA 510 mA 530 mA 490 mA 235 mA 170 mA 12.

9 W 6.8 W 6.6 W 1.4 W 1.0 W POWER Power Mode Definitions Spin-up The drive is spinning up following initial application of power and has not yet reached full speed. Seek A random access operation by the disk drive. Read/Write Data is being read from or written to the drive. Idle The drive is spinning, the actuator is parked and powered off and all other circuitry is powered on. The drive is capable of responding to read commands within 40 ms. Standby The spin motor is not spinning.

The drive will leave this mode upon receipt of a command that requires disk access. The time-out value for this mode is programmable. The buffer is active to accept write data. Sleep This is the lowest power state with the interface set to inactive. A software or hardware reset is required to return the drive to the Standby state. EPA Energy Star Compliance Maxtor Corporation supports the goals of the U.S. Environmental Protection Agency's Energy Star program to reduce the electrical power consumption of computer equipment. Environmental Limits PARAMETER Temperature OPERATING 5° C to 55° C NON-OPERATING/STORAGE low temperature (-40° C) high temperature (71° C) per MIL STD-810E, method 501.3, climatic category; hot-induced conditions. Thermal Gradient Relative Humidity Wet Bulb Altitude Acoustic Noise - Idle Mode (per ISO 7779, 10 microphone, average sound power) -200 to 10,000 feet 1 and 2 disk models: 3.6 bel 3 disk models: 3.7 bel 4 disk models: 3.8 bel 25° C per hour (maximum) 5% to 95% (non-condensing) 30° C (maximum) -200 to 40,000 feet 33 PRODUCT SPECIFICATIONS Shock and Vibration PARAMETER Mechanical Shock Rotational Shock Random Vibration OPERATING 60 Gs, 2.0 ms, no errors 10 - 45 Hz at 0.

004 G2/Hz 48 - 62 Hz at 0.008 G2/Hz 65 - 300 Hz at 0.004 G2/Hz 301 - 500 Hz at 0.0006 G2/Hz no errors NON-OPERATING 250 Gs, 2.0 ms, no damage 20,000 Rad/sec, 0.

5 - 1.0 ms, no damage 10 Hz at 0.05 G2/Hz 20 Hz at 0.055 G2/Hz 300 Hz at 0.05 G2/Hz 301 Hz at 0.0014 G2/Hz 500 - 760 Hz at 0.001 G2/Hz 877 Hz at 0.003 G2/Hz 1000 - 1570 Hz at 0.001 G2/Hz 2000 Hz at 0.001 G2/Hz Swept Sine Vibration 10 - 300 Hz 1.

0 G (0 - peak) amplitude Reliability Specifications Annual Return Rate < 1.0% Annual Return Rate (ARR) indicates the average against products shipped. ARR includes all reasons for returns (failures, handling damage, NDF), but does not include inventory credit returns. Quality Acceptance Rate < 1,000 DPPM The quality acceptance rate indicates the percentage of Maxtor products successfully installed by our customers, and/or the number of defective parts per million (DPPM) encountered during the entire installation process. Start/Stop Cycles 50,000 Data Reliability This indicates the average minimum cycles for reliable start/stop function. < 10 per 1015 bits read Data errors (non-recoverable). Average data error rate allowed with all error recovery features activated. Component Design Life 5 years (minimum) Component design life is defined as a.) the time period before identified wear-out mechanisms impact the failure rate, or b.) the time period up to the wear-out point when useful component life expires.

34 PRODUCT SPECIFICATIONS EMC/EMI Radiated Electromagnetic Field Emissions - EMC Compliance The hard disk drive mechanism is designed as a subassembly for installation into a suitable enclosure and is therefore not subject to Subpart J of Part 15 of FCC Rules (47CFR15) or the Canadian Department of Communications Radio Interference Regulations. Although not required, the disk mechanism has been tested within a suitable end-use product and found to comply with Class B limits of the FCC Rules and Regulations of the Canadian Department of Communications. The CE Marking indicates conformity with the European Union Low Voltage Directive (73/23/EEC) when the disk mechanism is installed in a typical personal computer. Maxtor recommends that testing and analysis for EMC compliance be performed with the disk mechanism installed within the user's end-use application. Canadian Emissions Statement This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus as set out in the radio interference regulations of the Canadian department of communications.

Le present appareil numerique n'emmet pas de bruit radioelectriques depassant les limites applicables aux appareils numeriques de Class B prescrites dans le reglement sur le brouillage radioelectrique edicte par le ministre des communications du Canada. Safety Regulatory Compliance All Maxtor hard drives comply with relevant product safety standards such as CE, CUL, TUV and UL rules and regulations. As delivered, Maxtor hard drives are designed for system integration before they are used. 35 INSTALLATION SECTION 4 Handling and Installation Hard Drive Handling Precautions N If the handling precautions are not followed, damage to the hard drive may result - which may void the warranty. N During handling, NEVER drop, jar, or bump a drive. Handle the drive by its sides and avoid touching the printed circuit board assembly (PCBA). N Hard drives are sensitive to electrostatic discharge (ESD) damage. Use proper ESD practices by grounding yourself and the computer system the hard drive will be installed in. N Allow the hard drive to reach room temperature BEFORE installing it in your computer system. N NEVER switch DC power onto the drive by plugging an electrically live DC source cable into the drive's connector. NEVER connect a live connector to the hard drive's IDE interface connector. N ELECTRICAL GROUNDING - For proper operation, the drive must be securely fastened to a device bay that provides a suitable electrical ground to the drive baseplate. Electro-Static Discharge (ESD) To avoid some of the problems associated with ESD, Maxtor advises that anyone handling a disk drive use a wrist strap with an attached wire connected to an earth ground. Failure to observe these precautions voids the product warranty. Manufacturers frequently experience "unsolved" component/hardware malfunctions often caused by ESD.

To reduce the incidence of ESD-related problems, Maxtor recommends that any electronics manufacturing plans include a comprehensive ESD program, the basic elements and functions of which are outlined here: ESD Program Element Management Chief coordinator Multi-department committee Employee training ESD Program Function Institute and maintain Organize and enforce Evaluate and improve Educate and inform ESD program supplies typically include: wrist- and foot-worn grounding straps; counter-top and floor antistatic matting; wrist strap testers; ESD video and training materials.



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Sources for such supplies include: Static Control Systems 3M 225-4S, 3M Center St. Paul, MN 55144 Charleswater 93 Border St. West Newton, MA 02165-9990 Maxtor also offers a complete video training package, "Care and Handling of Maxtor Disk Drives." Contact your Maxtor representative for details. 41 INSTALLATION Unpacking and Inspection Retain any packing material for reuse. Inspect the shipping container for evidence of damage in transit. Notify the carrier immediately in case of damage to the shipping container. As they are removed, inspect drives for evidence of shipping damage or loose hardware. If a drive is damaged (and no container damage is evident), notify Maxtor immediately for drive disposition.

Figure 4 - 1 Multi-pack Shipping Container 42 INSTALLATION Figure 4 - 2 Single Pack Shipping Container (Option A) Figure 4 - 3 Single Pack Shipping Container (Option B) Repacking If a Maxtor drive requires return, repack it using Maxtor packing materials, including the antistatic bag. Physical Installation Recommended Mounting Configuration The DiamondMax® drive design allows greater shock tolerance than that afforded by larger, heavier drives. The drive may be mounted in any attitude using four size 6-32 screws with 1/8-inch maximum penetration and a maximum torque of 5-inch pounds.

See Figure 3-1 for mounting dimensions. Allow adequate ventilation to the drive to ensure reliable operation.

See the following pages for specific installation steps. 43 INSTALLATION Before You Begin Important Please Read Please read this installation section completely before installing the Maxtor hard drive. It gives general information for installing a Maxtor hard drive in a typical computer system. If you don't understand the installation steps, have a qualified computer technician install the hard drive. Back up.

Protect your Existing Data Periodic backup of important data is always a good idea. Whenever your computer is on, there is the potential for losing data on your hard drive. This is especially true when running disk utilities or any software that directly manipulates your files. Maxtor recommends that you make a backup copy of the files on any existing hard drives prior to installing the new drive. If required, this data may then be copied to the Maxtor hard drive after it has been installed in the computer. Refer to your computer user's manual for detailed data backup instructions. Tools for Installation The following tools are needed to install your new Maxtor hard drive: · A small (#2) Phillips head screw driver · Small needle-nose pliers or tweezers · Your computer user's manuals · Operating system software System Requirements · IDE/AT interface Maxtor recommends: · Drives less than or equal to 8.4 GB 486 DX 66 MHz · Drives larger than 8.4 GB Pentium-class processor Operating System Requirements · Drives less than or equal to 8.4 GB: - DOS 5.

0 or higher · Drives larger than 8.4 GB: - Installing as boot drive (Primary Master) requires full installation set of Windows 95/98 not an update from DOS or Windows 3.x. - Installing as non-boot drive (Primary Slave, Secondary Master or Slave) requires Windows 95/98 on the boot drive. Hook up Maxtor recommends that you use the MaxBlast™ Plus software to create a customized installation guide for your system before physically installing your new hard drive. The information created by MaxBlast Plus relates to the following illustrations. Boot the System with the MaxBlast Plus Diskette Before physically installing the Maxtor hard drive, boot your system with the MaxBlast Plus diskette. It will assist you with the instructions in this section for a successful installation. Configure the Drive Jumpers The jumper configurations have three valid jumper settings Master, Slave and Cable Select. Maxtor hard drives are always shipped with the Master jumper setting enabled.

Install the 5.25-inch Mounting Brackets If the Maxtor hard drive will be mounted in a 5.25-inch device bay, you will need to attach 5.25-inch brackets to the hard drive. These brackets are not required if the drive is mounted in a 3.

5-inch device bay. 44 INSTALLATION Install the Hard Drive in a Device Bay Refer to your computer user's manual for specific mounting information. Be sure to secure the drive to the device bay with all four screws. Attach the Interface and Power Cables Do not force or rock the connectors into their sockets on the hard drive. Push them in straight until they are seated.

Note: DiamondMax Hard Drive Kits that carry a "U" in the kit number are UltraDMA 66 compatible hard drives. A standard IDE cable can be used for drive installation; however, an UltraDMA cable is required to achieve UltraDMA 66 data transfers in UltraDMA 66 compatible systems. Follow the illustration below for proper cable connections to the system and hard drive(s) when using this cable. Attach an IDE interface connector to J1 on the Maxtor drive. Attach a power connector to J2 on the Maxtor drive. This connector is keyed and will only fit one way. Check all other cable connections before you power up. Striped/colored edge is pin 1 After attaching the IDE interface cable and the power cable to the Maxtor hard drive, verify that all other cables connected to other devices, the mother board or interface card(s) are correctly seated. Striped/colored edge is pin Start up Turn your system ON. During the system start up sequence, run the SETUP (BIOS) program.

Newer systems usually display a message like "press DEL to enter Setup," showing how to access the SETUP (BIOS) program. Choose the device position where the Maxtor hard drive will be installed (Primary Master, Primary Slave, Secondary Master, Secondary Slave or their equivalents) and select the "Auto Detect" option. Save and exit the BIOS. The system will now boot. Boot to the MaxBlast™ Plus diskette. Set up MaxBlast™ Plus will guide you through the steps to prepare (partition and format) your new Maxtor hard drive. Once you have completed this step, your new Maxtor hard drive will be ready to use.

Note: Do not discard the MaxBlast Plus diskette once the installation is complete. The diskette contains Maxdiag, a diagnostic utility that is a separate program from the MaxBlast™ Plus installation software. 45 AT INTERFACE DESCRIPTION SECTION 5 AT Interface Description Interface Connector All DiamondMax® Plus 40 AT drives have a 40-pin ATA interface connector mounted on the PCBA.

The drive may connect directly to the host; or it can also accommodate a cable connection (maximum cable length: 18 inches). Striped Edge (Pin 1) Drive 1 - Slave (gray) System Connector (blue) Drive 0 - Master (black) Figure 5-1 Data Connector Pin Description Summary P IN 01 03 05 07 09 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 S IG N A L Reset DD7 DD6 DD5 DD4 DD3 DD2 DD1 DD0 G ro u n d DM ARQ DIOW -:STOP DIOR -:HDMARDY:HSTROBE IORDY:DDMARDY:DSTROBE DMACK IN T R Q DA1 DA0 CS0 DASP P IN 02 04 06 08 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 S IG N A L G ro u n d DD8 DD9 DD10 DD11 DD12 DD13 DD14 DD15 (keypin) G ro u n d G ro u n d G ro u n d CSEL G ro u n d IOCS16 O b s o l e t e PDIAG DA2 CS1 G ro u n d 51 AT INTERFACE DESCRIPTION Pin Description Table P IN N A M E RESET DD0 DD1 DD2 DD3 DD4 DD5 DD6 DD7 DD8 DD9 DD10 DD11 DD12 DD13 DD14 DD15 DM ARQ DIOW STOP D IO R HDMARDY HSTROBE IORDY DDMARDY DSTROBE CSEL DMACK IN T R Q IOCS16 PDIAG DA0 DA1 DA2 CS0 CS1 DASP GND 27 O I/O Channel Ready P IN 01 17 15 13 11 09 07 05 03 04 06 08 10 12 14 16 18 21 23 25 I/O O I I DMA Request Host I/O Write Host I/O Read This signal is used with DMACK for DMA transfers.



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By asserting this signal, the drive indicates that data is ready to be transferred to and from the host. Rising edge of Write strobe clocks data from the host data bus to a register on the drive. Read strobe enables data from a register on the drive onto the host data bus.

DMA ready during Ultra DMA data in bursts. Data strobe during Ultra DMA data out bursts. This signal may be driven low by the drive to insert wait states into host I/O cycles. **DMA ready during Ultra DMA data out bursts. Data strobe during Ultra DMA data in bursts.**

Used for Master/Slave selection via cable. Requires special cabling on host system and installation of Cable Select jumper. This signal is used with DMARQ for DMA transfers. By asserting this signal, the host is acknowledging the receipt of data or is indicating that data is available. Interrupt to the host asserted when the drive requires attention from the host. **Output by drive when in Slave mode; Input to drive when in Master mode.** 3 bit binary address from the host to select a register in the drive. **SIGNAL NAME Host Reset Host Data Bus SIGNAL DESCRIPTION** Reset signal from the host system. Active during power up and inactive after. 16 bit bi-directional data bus between host and drive.

Lower 8 bits used for register and ECC byte transfers. All 16 bits used for data transfers. 28 29 31 32 34 35 33 36 37 38 39 02 19 22 24 26 30 40 I/O 1 1 1 1 I/O N/A I/O Cable Select DMA Acknowledge Host Interrupt Request Device 16 bit I/O Passed Diagnostic Host Address Bus Host Chip Select 0 Host Chip Select 1 Drive Active/Drive 1 Present Ground Chip select from the host used to access the Command Block registers in the drive. This signal is a decode of I/O addresses 1F0 - 1F7 hex. Chip select from the host used to access the Control registers in the drive. This signal is a decode of I/O addresses 3F6 - 3F7 hex. Time-multiplexed, open collector output which indicates that a drive is active, or that device 1 is present. Signal ground. KEY 20 N/A Key Pin used for keying the interface connector. 52 AT INTERFACE DESCRIPTION PIO Timing TIMING PARAMETERS t0 t1 t2 t2 i t3 t4 t5 t6 t6 Z t9 tR dtA tB Cycle Time (min) Address valid to DIOR-/DIOW- setup (min) DIOR-/DIOW- 16-bit (min) DIOR-/DIOW- recovery time (min) DIOW- data setup (min) DIOW- data hold (min) DIOR- data setup (min) DIOW- data hold (min) DIOR- data t r i t a t e (max) DIOR-/DIOW- to address valid hold (min) Read Data Valid to IORDY active (min) IORDY Setup Time IORDY Pulse Width (max) 60 ns 30 ns 50 ns 5 ns 30 ns 20 ns 0 35 ns 1250 ns 45 ns 20 ns 35 ns 30 ns 15 ns 0 35 ns 1250 ns 30 ns 15 ns 20 ns 5 ns 30 ns 10 ns 0 35 ns 1250 ns M ODE 0 60 0 ns 70 ns 165 ns M ODE 1 383 ns 50 ns 125 ns M ODE 2 240 ns 30 ns 100 ns M ODE 3 180 ns 30 ns 80 ns 70 ns 30 ns 10 ns 20 ns 5 ns 30 ns 10 ns 0 35 ns 1250 ns M ODE 4 120 ns 25 ns 70 ns 25 ns 20 ns 10 ns 20 ns 5 ns 30 ns 10 ns 0 35 ns 1250 ns Figure 5 - 2 PIO Data Transfer To/From Device 53 AT INTERFACE DESCRIPTION DMA Timing TIMING PARAMETERS t0 tC tD tE tF tG tH tI tJ tK r tKw tL r tLw tZ Cycle Time (min) DMACK to DMARQ delay DIOR-/DIOW- (min) DIOR- data access (min) DIOR- data hold (min) DIOR-/DIOW- data setup (min) DIOW- data hold (min) DMACK to DIOR-/DIOW- setup (min) DIOR-/DIOW- to DMACK hold (min) DIOR- negated pulse width (min) DIOW- negated pulse width (min) DIOR- to DMARQ delay (max) DIOW- to DMARQ delay (max) DMACK- to tristate (max) 215 ns 150 ns 5 ns 100 ns 20 ns 0 20 ns 50 ns 215 ns 120 ns 40 ns 20 ns 80 ns 60 ns 5 ns 30 ns 15 ns 0 5 ns 50 ns 50 ns 40 ns 40 ns 25 ns 5 ns 20 ns 10 ns 0 5 ns 25 ns 25 ns 35 ns 35 ns 25 ns 70 ns M ODE 0 480 ns M ODE 1 150 ns M ODE 2 120 ns Figure 5 - 3 Multi-word DMA Data Transfer 54 AT INTERFACE DESCRIPTION Ultra DMA Timing TIMING PARAMETERS tCYC t2CYC tDS tDH tDVS tDVH tF S tLI tMLI tUI tAZ tZAH tZAD tENV tSR tRFS tRP tIORDYZ tZIORDY tACK tSS Cycle Time (from STROBE edge to STROBE edge) Two cycle time (from rising edge to next rising edge or from falling edge to next falling edge of STROBE) Data setup time (at recipient) Data hold time (at recipient) Data valid setup time at sender (time from data bus being valid until STROBE edge) Data valid hold time at sender (time from STROBE edge until data may go invalid) First STROBE (time for device to send first STROBE) Limited interlock time (time allowed between an action by one agent, either host or device, and the following action by the other agent) Interlock time with minimum Unlimited interlock time Maximum time allowed for outputs to release Minimum delay time required for output drivers turning on (from release state) Envelope time (all control signal transitions are within the DMACK envelope by this much time) STROBE to DMARDY (response time to ensure the synchronous pause case when the recipient is pausing) Ready-to-final-STROBE time (no more STROBE edges may be sent this long after receiving DMARDY- negation) Ready-to-pause time (time until a recipient may assume that the sender has paused after negation of DMARDY-) Pull-up time before allowing IORDY to be released Minimum time device shall wait before driving IORDY Setup and hold times before assertion and negation of DMACK Time from STROBE edge to STOP assertion when the sender is stopping 0 20 50 160 20 0 20 50 20 0 20 70 50 75 125 20 0 20 50 M ODE 0 M IN 112 230 15 5 70 6 0 0 20 0 10 20 0 20 70 30 70 100 20 0 20 50 230 150 M AX M ODE 1 M IN 73 154 10 5 48 6 0 0 20 0 10 20 0 20 70 20 60 100 20 0 20 50 20 0 150 M AX M ODE 2 M IN 54 115 7 5 30 6 0 0 20 0 10 20 0 20 55 NA 60 100 20 170 150 M AX M ODE 3 M IN 39 86 7 5 20 6 0 0 20 0 10 20 0 20 55 NA 60 130 100 M AX M ODE 4 M IN 25 57 5 5 6 6 0 0 20 0 10 120 100 M AX DMARQ (device) tUI DMACK(host) tACK STOP (host) tACK tENV tZAD tZIORDY DSTROBE (device) tAZ DD(15:0) tACK DA0, DA1, DA2, CS0-, CS1 tVDS tDVH tENV tZAD tFS tFS HDMARDY(host) Figure 5 - 4 Initiating an Ultra DMA Data In Burst 55 AT INTERFACE DESCRIPTION t2CYC tCYC DSTROBE at device tDVH DD(15:0) at device tDVS tDVH tDVS tDVH tCYC t2CYC DSTROBE at host tDH DD(15:0) at host tDS tDH tDS tDH Figure 5 - 5 Sustained Ultra DMA Data In Burst DMARQ (device) DMACK(host) STOP (host) tSR HDMARDY(host) tRFS DSTROBE (device) DD(15:0) (device) tRP Figure 5 - 6 Host Pausing an Ultra DMA Data In Burst 56 AT INTERFACE DESCRIPTION DMARQ (device) tMLI DMACK(host) tLI STOP (host) tLI HDMARDY(host) tSS DSTROBE (device) tIORDYZ tACK tLI tACK tZAH tAZ tDVS CRC tDVH DD(15:0) tACK DA0, DA1, DA2, CS0-, CS1 - Figure 5 - 7 Device Terminating an Ultra DMA Data In Burst DMARQ (device) tLI DMACK(host) tRP STOP (host) tACK HDMARDY(host) tRFS DSTROBE (device) tDVS DD(15:0) CRC tACK DA0, DA1, DA2, CS0-, CS1 tDVH tLI tMLI tIORDYZ tAZ tMLI tZAH tACK Figure 5 - 8 Host Terminating an Ultra DMA Data In Burst 57 AT INTERFACE DESCRIPTION DMARQ (device) DMACK(host) tUI tACK STOP (host) tZIORDY DDMARDY(device) tACK HSTROBE (host) tENV tLI tUI tDVS DD(15:0) (host) tACK DA0, DA1, DA2, CS0-, CS1 - tDVH Figure 5 - 9 Initiating an Ultra DMA Data Out Burst t2CYC tCYC HSTROBE at host tDVH DD(15:0) at host tDVS tDVH tDVS tDVH tCYC t2CYC HSTROBE at device tDH DD(15:0) at device tDS tDH tDS tDH Figure 5 - 10 Sustained Ultra DMA Data Out Burst 58 AT INTERFACE DESCRIPTION tRP DMARQ (device) DMACK(host) STOP (host) tSR DDMARDY(device) tRFS HSTROBE (host) DD(15:0) (host) Figure 5 - 11 Device Pausing an Ultra DMA Data Out Burst tLI DMARQ (device) tMLI DMACK(host) tSS STOP (host) tLI DDMARDY(device) tIORDYZ tLI tACK tACK HSTROBE (host) tDVS DD(15:0) (host) DA0, DA1, DA2, CS0-, CS1 tCRC tACK tDVH Figure 5 - 12 Host Terminating an Ultra DMA Data Out Burst 59 AT INTERFACE DESCRIPTION DMARQ (device) DMACK(host) tLI STOP (host) tRP DDMARDY(device) tRFS tLI HSTROBE (host) tDVS DD(15:0) (host) DA0, DA1, DA2, CS0-, CS1 tCRC tACK tDVH tMLI tACK tIORDYZ tMLI tACK Figure 5 - 13 Device Terminating an Ultra DMA Data Out Burst 5 10 HOST SOFTWARE INTERFACE SECTION 6 Host Software Interface The host communicates with the drive through a set of controller registers accessed via the host's I/O ports.



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These registers divide into two groups: the Task File, used for passing commands and command parameters and the Control/Diagnostic registers. Task File registers The Task File consists of eight registers used to control fixed disk operations. The host accesses each register by the I/O port address shown in this Task File register map: I/O P O R T 1F0h 1F1h 1F2h 1F3h 1F4h 1F5h 1F6h 1F7h READ Data Register Error Register S e c t o r C o u n t S e c t o r N u m b e r C y l i n d e r L o w C y l i n d e r H i g h D r i v e / H e a d (S D H) S t a t u s R e g i s t e r W R I T E D a t a R e g i s t e r F e a t u r e s R e g i s t e r S e c t o r C o u n t S e c t o r N u m b e r C y l i n d e r L o w C y l i n d e r H i g h D r i v e / H e a d (S D H) C o m m a n d R e g i s t e r D a t a R e g i s t e r P r o v i d e s a c c e s s t o t h e d r i v e ' s s e c t o r b u f f e r f o r r e a d a n d w r i t e o p e r a t i o n s . W i t h t h e e x c e p t i o n o f E C C b y t e t r a n s f e r s (w h i c h , d u r i n g R e a d l o n g a n d W r i t e l o n g c o m m a n d s , a r e 8 b i t s w i d e) , d a t a t r a n s f e r s t h r o u g h t h e D a t a r e g i s t e r a r e a l l 16 b i t s w i d e . E r r o r R e g i s t e r A r e a d - o n l y r e g i s t e r c o n t a i n i n g s p e c i f i c i n f o r m a t i o n r e g a r d i n g t h e p r e v i o u s c o m m a n d .

Data interpretation differs depending on whether the controller is in operational or diagnostic mode. A power up, reset, software reset, or receipt of a diagnostic command sets the controller into diagnostic mode. This mode invalidates contents of the Status register. The contents of the Error register reflect a completion code. Issuing any command (apart from a Diagnostic command) places the controller into operational mode.

In operational mode, the Error register is valid only when the Error bit in the Status register is set. The bit definitions for operational mode follow: 7 0 I n t e r f a c e C R C 6 E C C D a t a E C C E r r o r 5 0 N o t U s e d 4 I D N F I D N o t F o u n d 3 0 N o t U s e d 2 A B R T A b o r t e d C o m m a n d 1 T K 0 T r a c k 0 E r r o r 0 A M N F A d d r e s s M a r k N o t F o u n d I n t e r f a c e C R C A n i n t e r f a c e C R C e r r o r o c c u r r e d d u r i n g a n U l t r a D M A t r a n s f e r . D a t a E C C E r r o r A n n o n - c o r r e c t a b l e E C C e r r o r o c c u r r e d d u r i n g a R e a d S e c t o r c o m m a n d . F i r m w a r e P r o b l e m I n d i c a t e s a f i r m w a r e p r o b l e m w a s d e t e c t e d , (e . g . , i n v a l i d i n t e r r u p t , d i v i d e o v e r f l o w) . I D N o t F o u n d E i t h e r a m a t c h i n g I D f i e l d n o t f o u n d , o r a C R C e r r o r o c c u r r e d . A b o r t e d C o m m a n d I n v a l i d c o m m a n d s , w r i t e f a u l t , n o s e e k c o m p l e t e , o r d r i v e n o t r e a d y . T r a c k 0 E r r o r T r a c k 0 w a s n o t f o u n d d u r i n g e x e c u t i o n o f a R e s t o r e c o m m a n d . A d d r e s s M a r k N o t F o u n d T h e A d d r e s s M a r k c o u l d n o t b e f o u n d a f t e r a n I D m a t c h .

Features Register Enables or disables features through the Set Features command. 61 HOST SOFTWARE INTERFACE Sector Count Register Holds the number of sectors to be sent during a Read or Write command, and the number of sectors per track during a Format command. A value of zero in this register implies a transfer of 256 sectors. A multisector operation decrements the Sector Count register. If an error occurs during such an operation, this register contains the remaining number of sectors to be transferred. Sector Number Register Holds the starting sector number for any disk operation. The register is updated as each sector is processed in a multi-sector operation. Cylinder Number Registers Two 8-bit Cylinder Number registers (Low and High) specify the starting cylinder for disk operation. Device/Head Register Used to specify the drive and head number to be operated on during any disk operations. Within the context of a Set Parameters command, this register specifies the maximum number of heads on the drive.

Bit definitions follow: 7 1 6 L B A M o d e 5 1 4 D R V S e l e c t D r i v e 3 H S 1 S e l e c t 2 H S 2 H e a d S e l e c t 1 H S 1 H e a d S e l e c t 0 H S 0 H e a d S e l e c t S e l e c t L B A M o d e E n a b l i n g t h i s b i t f o r c o m m a n d s n o t s u p p o r t e d b y L B A m o d e w i l l a b o r t t h e s e l e c t e d c o m m a n d . W h e n s e t , t h e T a s k F i l e r e g i s t e r c o n t e n t s a r e d e f i n e d a s f o l l o w s f o r t h e R e a d / W r i t e a n d t r a n s l a t e c o m m a n d : C O N T E N T S S e c t o r N u m b e r C y l i n d e r L o w C y l i n d e r H i g h D r i v e / H e a d L B A B I T S 0 - 7 8 - 1 5 1 6 - 2 3 2 4 - 2 7 D r i v e S e l e c t S e t t o 0 t o s e l e c t t h e m a s t e r d r i v e ; s e t t o 1 t o s e l e c t t h e s l a v e d r i v e . H e a d S e l e c t S p e c i f i e s t h e b i n a r y c o d e d a d d r e s s o f t h e h e a d t o b e s e l e c t e d . S t a t u s R e g i s t e r C o n t a i n s r e s u l t s o f t h e l a s t c o m m a n d e x e c u t e d , a n d t h e d r i v e ' s s t a t u s . T h e o t h e r s e v e n T a s k F i l e r e g i s t e r s m a y b e r e a d o n l y w h e n b i t 7 (B U S Y) o f t h e S t a t u s r e g i s t e r i s l o w .

Reading any of the Task File registers when BUSY is high returns the value of the Status register. Reading the Status register also clears any interrupt request to the host. Bit definitions follow: 7 B U S Y C o n t r o l l e r B u s y 6 D R D Y D e v i c e R e a d y 5 D F D e v i c e F a u l t 4 D S C D e v i c e S e e k C o m p l e t e 3 D R Q D a t a R e q u e s t 2 0 1 0 0 E R R E r r o r C o n t r o l l e r B u s y G o e s a c t i v e w h e n a c o m m a n d i s w r i t t e n t o t h e C o m m a n d r e g i s t e r , i n d i c a t i n g c o n t r o l l e r t a s k e x e c u t i o n . A f t e r a c o m m a n d , t h i s b i t r e s e t s . D e v i c e R e a d y I n d i c a t e s t h a t t h e d r i v e i s r e a d y f o r c o m m a n d s .

If drive ready is not present, all commands abort. Device Fault Indicates the drive's detection of a write fault condition, causing all commands to abort. Device Seek Complete Signifies a seek completion, and that the drive is on track. Data Request Indicates that the drive's sector buffer is ready for data transfer. Error The Error bit sets when the previous command has completed with a non-recoverable error. 62 HOST SOFTWARE INTERFACE Command Register Contains code for the command to be performed. Additional command information should be written to the task file before the Command register is loaded. When this register is written, the BUSY bit in the Status register sets, and interrupt request to the host clears; invalid commands abort. (Detailed information on interface commands is given in Section 7.) Hex values for valid command formats follow: Read Commands Read Sector(s) Read Verify Sector(s) Read Sector Buffer Read Multiple Read DMA 20h 21h 22h 23h 40h 41h E4h C4h C9h Normal reads; retries enabled Normal reads; retries disabled Read Long; retries enabled Read Long; retries disabled Retries enabled Retries disabled C8h No retries Write Commands Write Sector(s) Write Write Write Verify Sector(s) Sector Buffer Multiple DMA 30h 31h 32h 33h 3Ch E8h C5h CAh CBh Normal writes; retries enabled Normal writes; retries disabled Write Long; retries enabled Write Long; retries disabled No retries Mode Set/Check Commands Set Features Set Multiple Mode Power Mode Commands EFh C6h Standby Immediate Idle Immediate Standby Idle Check Power Mode Set Sleep Mode Initialization Commands 94/E0h 95/E1h 96/E2h 97/E3h 98/E5h 99/E6h Stops Starts Stops Starts drive spindle; do not change time-out value spindle; do not change time-out value spindle; change time-out value spindle; change time-out value Identify Drive Initialize Drive Parameters Re-calibrate ECh 91h 1xh Seek, Format, and Diagnostic Commands Seek Format Track Execute Drive Diagnostic S.

M.A.R.T. Commands 7xh 50h 90h Execute S.



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M.A.R.T. B0h 63 HOST SOFTWARE INTERFACE Summary CO M M A N D N A M E Recalibrate Read Sector(s) Read DMA Write Sector(s) Write DMA Write Verify Sector(s) Read Verify Sector(s) Format Track Seek Execute Diagnostic Initialize Parameters Read Sector Buffer Write Sector Buffer Identify Drive Set Features Read Multiple Write Multiple S e t M u l t i p l e M o d e C O M M A N D C O D E b70010100001111111111b60010101110011111111b5010101001001111000b4100101011110000000b3x0101100x000111000b2x0000100x001011111b1xL0L1000x000001001b0xxxxx0x0x010001010 PARAMETERS USED F N S C N Y Y Y Y Y Y Y N N N N Y N N N N Y Y Y S N N Y Y Y Y Y Y N Y N N N N N N Y N C N Y Y Y Y Y Y Y Y N N N N N N N Y N S D H D Y Y Y Y Y Y Y D Y D D D D Y Y D T I M E - O U T P E R I O D T i m e - o u t d i s a b l e d (v a l u e * 5) s e c o n d s ((v a l u e - 2 4 0) * 3 0) m i n u t e s 2 1 m i n u t e s V e n d o r u n i q u e p e r i o d = 1 0 h o u r s R e s e r v e d 2 1 m i n u t e s , 1 5 s e c o n d s 6 4 H O S T S O F T W A R E I N T E R F A C E C o n t r o l D i a g n o s t i c R e g i s t e r s T h e s e I / O p o r t a d d r e s s e s r e f e r e n c e t h r e e C o n t r o l / D i a g n o s t i c r e g i s t e r s : I / O P O R T 3 F 6 h 3 F 7 h R E A D A l t e r n a t e S t a t u s D i g i t a l I n p u t W R I T E F i x e d D i s k C o n t r o l N o t u s e d A l t e r n a t e S t a t u s R e g i s t e r C o n t a i n s t h e s a m e i n f o r m a t i o n a s t h e S t a t u s r e g i s t e r i n t h e T a s k F i l e .

However, this register may be read at any time without clearing a pending interrupt. Device Control Register Contains the software Reset and Enable bit to enable interrupt requests to the host. Bit definitions follow: 7 0 6 0 5 0 4 0 3 0 2 SRST Reset 1 I E N I R Q E n a b l e 0 0 Reset Setting the software Reset bit holds the drive in the reset state. Clearing the bit re-enables the drive. The software Reset bit must be held active for a minimum of 5 µsec. IRQ Enable Setting the Interrupt Request Enable to 0 enables the IRQ 14 signal to the host. When this bit is set to 1, IRQ14 is tri-stated, and interrupts to the host are disabled. Any pending interrupt occurs when the bit is set to 0. The default state of this bit after power up is 0 (interrupt enabled). Digital Input Register Contains information about the state of the drive.

Bit definitions follow: 7 x Reser ved 6 -W G G a t e 5 -H S 3 H e a d S e l e c t 3 4 -H S 2 H e a d S e l e c t 2 3 -H S 1 H e a d S e l e c t 1 2 -H S 0 H e a d S e l e c t 0 1 -D S 1 D r i v e S e l e c t 1 0 D S 0 D r i v e S e l e c t 0 B i t 7 o f t h e h o s t d a t a b u s i s n o t d r i v e n w h e n t h i s r e g i s t e r i s r e a d . -W r i t e G a t e R e f l e c t s t h e s t a t e o f t h e a c t i v e l o w w r i t e g a t e s i g n a l o n t h e d r i v e . -H e a d S e l e c t 3 t h r o u g h -H e a d S e l e c t 0 R e p r e s e n t s t h e o n e s c o m p l e m e n t o f t h e c u r r e n t l y s e l e c t e d h e a d n u m b e r . -D r i v e S e l e c t 1 I s 0 i f d r i v e 1 s e l e c t e d ; 1 o t h e r w i s e . -D r i v e S e l e c t 0 I s 0 i f d r i v e 0 s e l e c t e d ; 1 o t h e r w i s e . 6 5 H O S T S O F T W A R E I N T E R F A C E R e s e t a n d I n t e r r u p t H a n d l i n g R e s e t H a n d l i n g O n e o f t h r e e d i f f e r e n t c o n d i t i o n s m a y c a u s e a r e s e t : p o w e r o n , h a r d w a r e r e s e t o r s o f t w a r e r e s e t . A l l t h r e e c a u s e t h e i n t e r f a c e p r o c e s s o r t o i n i t i a l i z e i t s e l f a n d t h e T a s k F i l e r e g i s t e r s o f t h e i n t e r f a c e . A r e s e t a l s o c a u s e s a s e t o f t h e B u s y b i t i n t h e S t a t u s r e g i s t e r . T h e B u s y b i t d o e s n o t c l e a r u n t i l t h e r e s e t c l e a r s a n d t h e d r i v e c o m p l e t e s i n i t i a l i z a t i o n . C o m p l e t i o n o f a r e s e t o p e r a t i o n d o e s n o t g e n e r a t e a h o s t i n t e r r u p t .

Task File registers are initialized as follows: Error Sector Count Sector Number Cylinder Low Cylinder High Drive/Head 1 1 1 0 0 0 Interrupt Handling The drive requests data transfers to and from the host by asserting its IRQ 14 signal. This signal interrupts the host if enabled by bit 1 (IRQ enable) of the Fixed Disk Control register. Clear this interrupt by reading the Status register, writing the Command register, or by executing a host hardware or software reset. 66 INTERFACE COMMANDS SECTION 7 Interface Commands The following section describes the commands (and any parameters necessary to execute them), as well as Status and Error register bits affected. Read Commands Read Sector(s) Read Verify Sector(s) Read Sector Buffer Read DMA Multi-word DMA Ultra DMA Read Multiple Set Multiple Write Commands Write Sector(s) Write Verify Sector(s) Write Sector Buffer Write DMA Multi-word DMA Ultra DMA Write Multiple Set Feature Commands Set Features Mode Power Mode Commands Standby Immediate Idle Immediate Standby Idle Check Power Mode Set Sleep Mode Default Power-on Condition Initialization Commands Identify Drive Initialize Drive Parameters 71 INTERFACE COMMANDS Read Commands Read Sector(s) Reads from 1 to 256 sectors, as specified in the Command Block, beginning at the specified sector. (A sector count of 0 requests 256 sectors.) Immediately after the Command register is written, the drive sets the BSY bit and begins execution of the command. @@Once at the desired track, the drive searches for the data address mark of the requested sector. The data address mark must be recognized within a specified number of bytes, or the Data Address Mark Not Found error will be reported. Assuming the data address mark is found: 1.

2. 3. 4. The data field is read into the sector buffer. Error bits are set (if an error was encountered).

The DRQ bit is set. An interrupt is generated. The DRQ bit is always set, regardless of the presence or absence of an error condition after the sector. Upon command completion, the Command Block registers contain the numbers of the cylinder, head and sector of the last sector read. Back-to-back sector read commands set DRQ and generate an interrupt when the sector buffer is filled at the completion of each sector.

The drive is then ready for the data to be read by the host. DRQ is reset and BSY is set immediately when the host empties the sector buffer. If an error occurs during Read Sector commands, the read terminates at the sector where the error occurred. The host may then read the Command Block to determine the nature of that error, and the sector where it happened. If the error type is a correctable or a non-correctable data error, the flawed data is loaded into the sector buffer. A Read Long command sets the Long bit in the command code and returns the data and the ECC bytes in the data field of the specified sector. During a Read Long, the drive does not check the ECC bytes to determine if there has been a data error. The Read Long command is limited to single sector requests. Read Verify Sector(s) Identical to the Read Sector(s) command, except that: 1. DRQ is never set, 2.

No data is transferred back to the host and 3. The long bit is not valid. 72 INTERFACE COMMANDS Read DMA Multi-word DMA Identical to the Read Sector(s) command, except that 1. The host initializes a slave-DMA channel prior to issuing the command, 2. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel and 3.



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The drive issues only one interrupt per command to indicate that data transfer has terminated and status is available. Ultra DMA With the Ultra DMA Read protocol, the control signal (DSTROBE) that latches data from DD(15:0) is generated by the devices which drives the data onto the bus. Ownership of DD(15:0) and this data strobe signal are given DSTROBE to the drive during an Ultra DMA data in burst. During an Ultra DMA Read burst, the drive always moves data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a DSTROBE edge to latch the data. Both edges of DSTROBE are used for data transfers.

Any unrecoverable error encountered during execution of a Read DMA command terminates data transfer after the transfer of all sectors prior to the sector where the error was detected. The sector in error is not transferred. The drive generates an interrupt to indicate that data transfer has terminated and status is available. The error posting is identical to the Read Sector(s) command. Read Multiple Performs similarly to the Read Sector(s) command, except that for each READ MULTIPLE command data transfers are multiple sector blocks and the Long bit is not valid.

Execution is also similar to that of the READ SECTOR(S) command, except that: 1. Several sectors are transferred to the host as a block, without intervening interrupts. 2. DRQ qualification of the transfer is required only at the start of each block, not of each sector. The block count consists of the number of sectors to be transferred as a block.

(The block count is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command.) READ LONG command is limited to single sector requests. When the Read Multiple command is issued, the Sector Count register contains the number of sectors requested -- not the number of blocks or the block count. If the number of sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. This final, partial block transfer is for N sectors, where $N = (\text{sector count}) \text{ modulo } (\text{block count})$ The Read Multiple operation will be rejected with an Aborted Command error if attempted: 1. Before the Set Multiple Mode command has been executed, or 2. When Read Multiple commands are disabled. The controller reports disk errors encountered during Read Multiple commands at the start of the block or partial block transfer. However, DRQ still sets, and the transfer occurs normally, along with the transfer of any corrupt data. Remaining block data from the following the sector in error is not valid.

If the Sector Count register contains 0 when the Set Multiple Mode command is issued, Read Multiple and Write Multiple commands are disabled; no error is returned. Once the appropriate action has been taken, the controller resets BSY and generates an interrupt. At power up, or after a hardware or software reset, Read Multiple and Write Multiple commands are disabled by default. 73 INTERFACE COMMANDS Set Multiple Mode Enables the controller to perform Read and Write Multiple operations, and establishes the block count for these commands. @@The drives support block sizes of 2, 4, 8 and 16 sectors. @@@@After the host fills the buffer, DRQ is reset and BSY is set. @@@@When this command is received, the drive: 1. 2. 3. 4.

5. @@A disk write task begins to store the host data to disk. @@@@The controller sets BSY immediately upon receipt of the command, 2. Data transfers are multiple sector blocks and 3. The Long bit and Retry bit is not valid.

Command execution differs from Write Sector(s) because: 1. Several sectors transfer to the host as a block without intervening interrupts. 2. DRQ qualification of the transfer is required at the start of the block, not on each sector. The block count consists of the number of sectors to be transferred as a block and is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count register contains the number of sectors requested -- not the number of blocks or the block count. If the number of sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. This final, partial block transfer is for N sectors, where $N = (\text{sector count}) \text{ modulo } (\text{block count})$ The Write Multiple operation will be rejected with an Aborted Command error if attempted: 1. Before the Set Multiple Mode command has been executed, or 2. When Write Multiple commands are disabled. All disk errors encountered during Write Multiple commands report after the attempted disk write of the block or partial block in which the error occurred. The write operation ends with the sector in error, even if it was in the middle of a block. When an error occurs, subsequent blocks are not transferred. When DRQ is set at the beginning of each full and partial block, interrupts are generated. Write DMA Multi-word DMA Identical to the Write Sector(s) command, except that: 1.

2. 3. The host initializes a slave-DMA channel prior to issuing the command, Data transfers are qualified by DMARQ and are performed by the slave-DMA channel and The drive issues only one interrupt per command to indicate that data transfer has terminated at status is available. Ultra DMA With the Ultra DMA Write protocol, the control signal (HSTROBE) that latches data from DD(15:0) is generated by the devices which drives the data onto the bus.

Ownership of DD(15:0) and this data strobe signal are given to the host for an Ultra DMA data out burst. During an Ultra DMA Write burst, the host always moves data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a HSTROBE edge to latch the data. Both edges of HSTROBE are used for data transfers. Any error encountered during Write DMA execution results in the termination of data transfer. The drive issues an interrupt to indicate that data transfer has terminated and status is available in the error register. The error posting is the same as that of the Write Sector(s) command.

75 INTERFACE COMMANDS Set Feature Commands Set Features Mode Enables or disables features supported by the drive. When the drive receives this command it: 1. 2. 3. 4.

Sets BSY, Checks the contents of the Features register, Clears BSY and Generates an interrupt. If the value of the register is not a feature supported by the drive, the command is aborted. The acceptable values in the Features register are defined as follows: VALUE 02h* 03h 44h 55h 66h* 82h AAh* BBh* CCh D

E S C R I P T I O N Enabled write cache Set transfer mode based on value in Sector Count register Length of data appended on Read Long/Write Long commands specified in the Identify Device information Disable read look-ahead feature Disable reverting to power-on defaults Disable write cache Enable read look-ahead feature 4 bytes of Maxtor specific data appended on Read Long/Write Long commands Enable reverting to power-on defaults * Enabled at power up by default.



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